BROADCOM®

Data Sheet

ACPL-736J

Optically Isolated ±50-mV Sigma-Delta Modulator with CMOS Interface

Description

The Broadcom® ACPL-736J is a 1-bit, second-order sigma-delta (Σ-Δ) modulator that oversamples an analog input signal into a high-speed data stream with galvanic isolation based on optical coupling technology. The ACPL-736J operates from a 5V power supply with a dynamic range of 80 dB with an appropriate digital filter. The differential inputs of ±50 mV (full scale of ±80 mV) are ideal for direct connection to shunt resistors or other low-level signal sources in applications such as motor phase current measurement.

The analog input is continuously sampled by means of sigma-delta oversampling using an external clock coupled across the isolation barrier, which allows synchronous operation with any digital controller. The signal information is contained in the modulator data as a density of ones with a data rate up to 21 MHz, and the data is encoded and transmitted across the isolation boundary where it is recovered and decoded into a high-speed data stream of digital ones and zeros. The original signal information can be reconstructed with a digital filter. For better signal integrity, the ACPL-736J comes with a CMOS interface on both clock inputs and data outputs.

Combined with superior optical coupling technology, the modulator delivers high noise margins and excellent immunity against isolation-mode transients. With a 0.5-mm minimum distance through insulation (DTI), the ACPL-736J provides reliable double protection and high working insulation voltage, which is suitable for fail-safe designs. This outstanding isolation performance is superior to alternatives including devices based on capacitive or magnetic coupling with DTI in the micro-meter range. Offered in an SO-16 package, the isolated ADC delivers the reliability, small size, superior isolation, and over-temperature performance that motor drive designers need to accurately measure current, at a much lower price compared to traditional current transducers.

Features

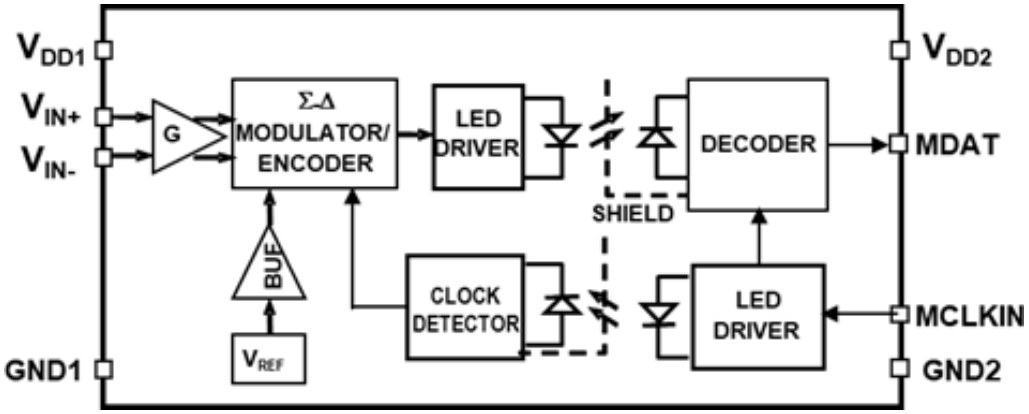
- External clock input range of 5 MHz to 21 MHz
- CMOS clock and data interface
- 1-bit, second-order sigma-delta modulator
- 16-bit resolution; no missing codes (12 bits ENOB)
- Typical SNR of 81 dB and typical SNDR of 80 dB
- Maximum offset drift of –2 µV/°C to 1 µV/°C
- Maximum gain error of ±1%
- Linear range of ±50 mV with a single 5V supply (full-scale range of ±80 mV)
- Operating temperature range of –40°C to +110°C
- SO-16 package
- Common-mode transient immunity of 80 kV/µs
- Safety and regulatory approval:
  - IEC/EN 60747-5-5: working insulation voltage of 1414 Vpeak
  - UL 1577: double protection rating of 5000 V_{rms}/1 min.
  - CAN/CSA-C22.2 No. 62368-1

Applications

- Motor phase and rail current sensing
- Power inverter current sensing
- Industrial process control
- Data acquisition systems
- General-purpose current sensing
- Traditional current transducer replacement

CAUTION! Take normal static precautions in the handling and assembly of this component to prevent damage, degradation, or both that may be induced by electrostatic discharge (ESD). The component featured in this data sheet is not recommended to be used in military or aerospace applications or environments. The component is also not AEC-Q100 qualified and not recommended for automotive applications.

Functional Block Diagram



Pin Configuration and Descriptions

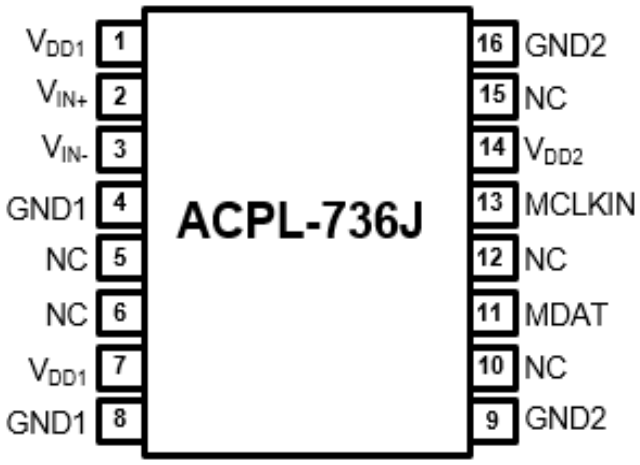


Table 1: Pin Descriptions

Pin No.	Symbol	Description
1, 7	V_{DD1}	Supply voltage for the input side relative to GND1. Pin 1 and 7 are *not* internally connected so they must be externally connected together to V_{DD1}.
2	V_{IN+}	Positive analog input; recommended input range ±50 mV.
3	$V_{IN–}$	Negative analog input; recommended input range ±50 mV (normally connected to GND1).
4, 8	GND1	Supply ground for signal input side.
5, 6, 10, 12, 15	NC	Leave the pins unconnected. Do not connect to V_{DD1}, GND1 or V_{DD2}, GND2.
9, 16	GND2	Supply ground for data output side (digital side).
11	MDAT	Modulator data output.
13	MCLKIN	Modulator clock input.
14	V_{DD2}	Supply voltage for output side, referenced to GND2.

Table 2: Ordering Information

Part Number	Option (RoHS Compliant)	Package	Tape and Reel	IEC/EN 60747-5-5	Quantity
ACPL-736J	-000E	SO-16		X	45 per tube
	-500E		X	X	850 per reel

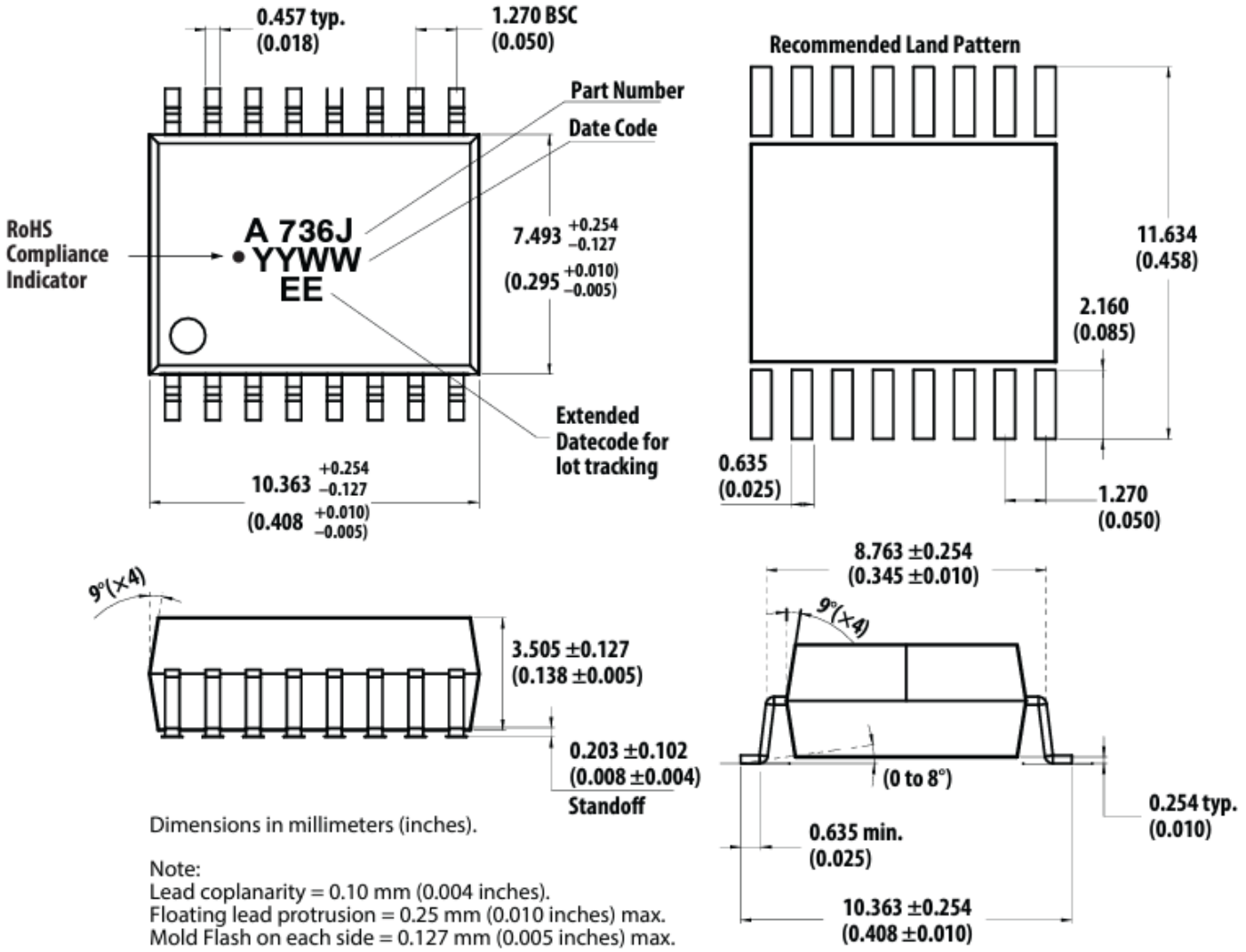
To form an order entry, choose a part number from the Part Number column and combine it with the desired option from the Option column.

Example: Use ACPL-736J-500E to order the product in tape and reel packaging.

Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawings

Figure 1: 16-Lead Surface Mount (SO-16)



Dimensions in millimeters (inches).

Note:
Lead coplanarity = 0.10 mm (0.004 inches).
Floating lead protrusion = 0.25 mm (0.010 inches) max.
Mold Flash on each side = 0.127 mm (0.005 inches) max.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The ACPL-736J is approved by the following organizations:

IEC/EN 60747-5-5	Approved with maximum working insulation voltage V_{IORM} = 1414 Vpeak.
UL	Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{rms}/1 minute. File E55361.
CSA	Approval under CAN/CSA-C22.2 No. 62368-1

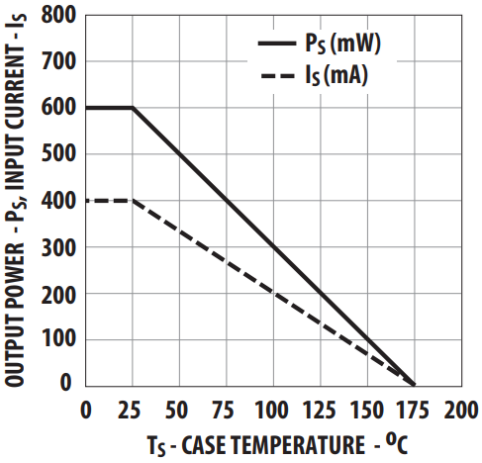
IEC/EN 60747-5-5 Insulation Characteristics[a]

Description	Symbol	Value	Unit
Installation classification per DIN VDE 0110/1.89, Table 1 For Rated Mains Voltage ≤ 150 V_{rms} For Rated Mains Voltage ≤ 300 V_{rms} For Rated Mains Voltage ≤ 450 V_{rms} For Rated Mains Voltage ≤ 600 V_{rms} For Rated Mains Voltage ≤ 1000 V_{rms}	—	 I-IV I-IV I-IV I-IV I-III	—
Climatic Classification	—	55/110/21	—
Pollution Degree (DIN VDE 0110/1.89)	—	2	—
Maximum Working Insulation Voltage	V_{IORM}	1414	Vpeak
Input to Output Test Voltage, Method b V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 second, Partial Discharge < 5 pC	V_{PR}	2652	Vpeak
Input to Output Test Voltage, Method a V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, Partial Discharge < 5 pC	V_{PR}	2262	Vpeak
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60 seconds)	V_{IOTM}	8000	Vpeak
Safety-Limiting Values (maximum values allowed in the event of a failure) Case Temperature Input Current[b] Output Power[b]	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 175 400 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	≥10^9	Ω

a. Insulation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits within the application.

b. Safety-limiting parameters are dependent on ambient temperature. See Figure 2 for dependence of P_S and I_S on ambient temperature.

Figure 2: Case Temperature Chart



Insulation and Safety Related Specifications

Parameter	Symbol	Conditions	Value	Unit
Minimum External Air Gap (External Clearance)	L(101)	Measured from input terminals to output terminals, shortest distance through air.	8.3	mm
Minimum External Tracking (External Creepage)	L(102)	Measured from input terminals to output terminals, shortest distance path along body.	8.3	mm
Minimum Internal Plastic Gap (Internal Clearance)	—	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and the photodetector inside the optocoupler cavity.	0.5	mm
Tracking Resistance (Comparative Tracking Index)	CTI	DIN IEC 112/VDE 0303 Part 1.	>175	V
Isolation Group	—	Material Group (DIN VDE 0110, 1/89, Table 1).	IIIa	—

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	–55	+125	°C
Junction Temperature	T_J	—	+125	°C
Ambient Operating Temperature	T_A	–40	+110	°C
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	6.0	V
Steady-State Input Voltage[a, b]	V_{IN+}, $V_{IN–}$	–2	V_{DD1} + 0.5	V
Two-Second Transient Input Voltage[c]	V_{IN+}, $V_{IN–}$	–6	V_{DD1} + 0.5	V
Digital Input/Output Voltages	MCLKIN, MDAT	–0.5	V_{DD2} + 0.5	V
Input Power Dissipation	P_{IN}	—	121	mW
Output Power Dissipation	P_O	—	82.5	mW
Total Power Dissipation	P_T	—	203.5	mW
Lead Solder Temperature	260°C for 10 seconds, 1.6 mm below seating plane			

a. DC voltage of up to –2V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.

b. Absolute maximum DC current on the inputs = 100 mA; no latch-up or device damage occurs.

c. Transient voltage of 2 seconds up to –6V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Ambient Operating Temperature	T_A	–40	+110	°C
V_{DD1} Supply Voltage	V_{DD1}	4.5	5.5	V
V_{DD2} Supply Voltage	V_{DD2}	3.0	5.5	V
Analog Input Voltage[a]	V_{IN+}, $V_{IN–}$	–50	+50	mV

a. Full-scale signal input range ±80 mV.

Electrical Specifications

Unless otherwise noted, T_A = –40°C to +110°C, V_{DD1} = 4.5V to 5.5V, V_{DD2} = 3.0V to 5.5V, V_{IN+} = –50 mV to +50 mV, and V_{IN-} = 0V (single-ended connection); tested with a Sinc3 filter, 256 decimation ratio, f_{MCLKIN} = 20 MHz.

Parameters	Symbol	Test Conditions	Min.	Typ.[a]	Max.	Unit	Notes	Figure
Static Characteristics								
Resolution	—	Decimation filter output set to 16 bits.	16	—	—	Bits		
Integral Nonlinearity	INL	T_A = –40°C to +110°C; see Definitions.	–16	—	16	LSB		
Differential Nonlinearity	DNL	No missing codes, guaranteed by design; see Definitions.	–0.9	—	0.9	LSB		
Input Offset Voltage	V_{OS}	T_A = 25°C, R_{SENSE} = 0Ω	–1	0.0	1	mV		7, 8, 9
Input Offset Voltage vs. Temperature	TCV_{OS}	T_A = –40°C to +110°C, V_{DD1} = 5V, R_{SENSE} = 0Ω	–2.0	–0.4	1.0	µV/°C		7
Input Offset Drift vs. V_{DD1}	—	—	—	100	—	µV/V		8
Internal Reference Voltage	V_{REF}	—	—	80	—	mV		
Gain Error	G_E	T_A = –40°C to +110°C, V_{IN+} = –50 mV to +50 mV; see Definitions.	–2	—	2	%		10, 11, 12
		T_A = 25°C, V_{IN+} = –50 mV to +50 mV	–1	—	1	%		10, 11, 12
Gain Error Drift vs. Temperature	TC_{GE}	T_A = –40°C to +110°C	—	±60	—	ppm/°C		10
Gain Drift vs. V_{DD1}	—	T_A = 25°C	—	–0.2	—	mV/V	b	12
Analog Inputs								
Linear-Scale Input Differential Voltage Range	LSR	—	—	±50	—	mV		
Full-Scale Input Differential Voltage Range	FSR	Referenced to GND1.	—	±80	—	mV	c	
Input Common Mode Voltage Range	V_{ICM}	—	—	–0.2 to 2.5	—	V		
Input Bias Current	I_{INA}	V_{IN+} = 0V	—	–200	—	µA		
Input Resistance	R_{IN}	Across V_{IN+} or $V_{IN–}$ to GND1	—	2.0	—	kΩ		
Input Capacitance	C_{INA}	Across V_{IN+} or $V_{IN–}$ to GND1	—	8	—	pF		

Parameters	Symbol	Test Conditions	Min.	Typ.[a]	Max.	Unit	Notes	Figure
AC Characteristics								
Signal-to-Noise Ratio	SNR	T_A = –40°C to +110°C, V_{IN+} = 100 mVpp, 1-kHz sine wave; f_{MCLKIN} = 9 MHz to 21 MHz; see Definitions.	76	81	—	dB	d	13, 15
		T_A = –40°C to +110°C, V_{IN+} = 100 mVpp, 1-kHz sine wave; f_{MCLKIN} = 5 MHz to < 9 MHz; see Definitions.	74	81	—	dB	d	
Signal-to-(Noise + Distortion) Ratio	SNDR	T_A = –40°C to +110°C, V_{IN+} = 100 mVpp, 1-kHz sine wave; f_{MCLKIN} = 9 MHz to 21 MHz; see Definitions.	75	80	—	dB	e	14, 16
		T_A = –40°C to +110°C, V_{IN+} = 100 mVpp, 1-kHz sine wave; f_{MCLKIN} = 5 MHz to < 9 MHz; see Definitions.	73	80	—	dB	e	
Effective Number of Bits	ENOB	See Definitions.	—	12	—	Bits		
Isolation Transient Immunity	CMTI	T_A = 25°C	50	80	—	kV/µs	f	
Digital Inputs and Outputs								
Input High Voltage	V_{IH}	—	0.8 × V_{DD2}	—	—	mV	e	
Input Low Voltage	V_{IL}	—	—	—	0.2 x V_{DD2}	mV	e	
Output High Voltage	V_{OH}	V_{DD2} = 5V, I_{OUT} = –4 mA	V_{DD2} – 0.4	V_{DD2} – 0.2	—	V		
		V_{DD2} = 3.3V, I_{OUT} = –4 mA	V_{DD2} – 0.3	V_{DD2} – 0.15	—	V		
Output Low Voltage	V_{OL}	I_{OUT} = +4mA	—	—	0.4	V		
Power Supply								
Input Side Supply Current	I_{DD1}	V_{IN+} = –80 mV to +80 mV	—	17	22	mA		17, 18
Output Side Supply Current	I_{DD2}	V_{DD2} = 3.3V	—	10	12	mA		
		V_{DD2} = 5V	—	12	15	mA		19, 20

a. All typical values are under typical operating conditions at T_A = 25°C, V_{DD1} = 5V, V_{DD2} = 3.3V.

b. Gain error drift vs. V_{DD1} can be expressed as –0.25% / V with reference to V_{REF}.

c. Beyond the full-scale input range, the data output is either all zeros or all ones.

d. Input signal, sine wave, 100 mVpp, frequency = 1 kHz.

e. Ensured by design.

f. Bypass capacitors must be connected near Pin 1– Pin 4 and Pin 7– Pin 8.

Timing Specifications

Unless otherwise noted, T_A = –40°C to +110°C, V_{DD1} = 4.5V to 5.5V, V_{DD2} = 3.0V to 5.5V.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Notes	Figure
Modulator Clock Input Frequency	f_{MCLKIN}	Clock duty cycle 40% to 60%	5	—	21	MHz	a	
Data Hold Time after MCLKIN Rising Edge	T_H	CL = 15 pF	10	—	25	ns	b	3
Data Rising Time	T_R	CL = 15 pF	—	4	—	ns		
Data Falling Time	T_F	CL = 15 pF	—	7	—	ns		
Data (Valid) Delay upon MCLKIN Input Startup	T_{CS}	V_{IN} = 0V, V_{DD1} = 5V and V_{DD2} = 3.3V, T_A = 25°C	—	25	—	µs	c	4
Data (Valid) Delay upon V_{DD1} Power-Up	T_{PS1}	V_{IN} = 0V, V_{DD1} step up to 4.5V, V_{DD2} > 3.0V supplied, MCLKIN active, T_A = 25°C	—	40	—	µs	d, e	5
Data (Valid) Delay upon V_{DD2} Power-Up	T_{PS2}	V_{IN} = 0V, V_{DD1} > 4.5V, V_{DD2} step up to 3.0V, MCLKIN active, T_A = 25°C	—	60	—	µs	d, e	6

a. The ACPL-736J has an in-built clock conditioning scheme that makes it tolerant to variations in the input clock duty cycle.

b. Data setup time (T_S) before the rising edge of MCLKIN depends on the external clock frequency. For a 20-MHz clock frequency, it is recommended to sample the data using the MCLKIN rising edge.

c. Bypass capacitors of 10 µF in parallel with 0.1 µF are placed between V_{DD1} and GND1 and between V_{DD2} and GND2.

d. When V_{DD1} is not supplied, MDAT is high and the modulator output level is 1.

e. The test is done based on a 0.1-µF bypass cap at VDD1.

Figure 3: Data to Clock Timing

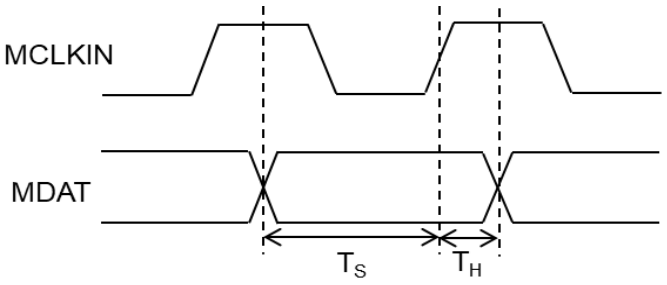


Figure 4: Data Delay upon Clock Input Startup

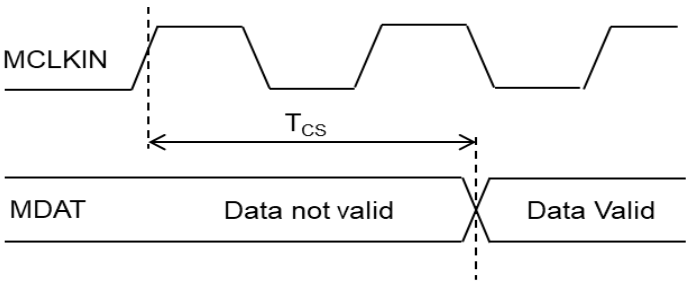


Figure 5: Data (Valid) Delay upon V_{DD1} Startup

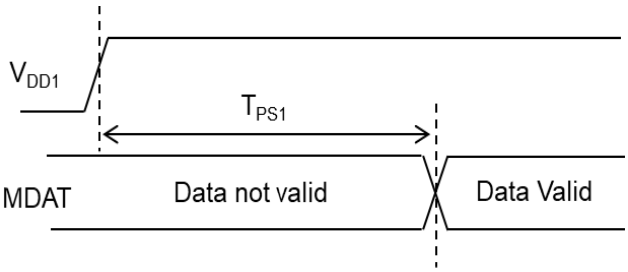
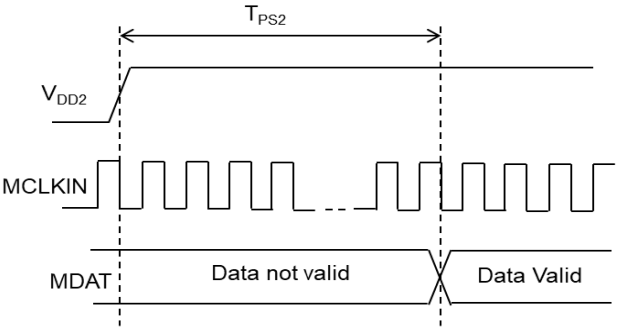


Figure 6: Data (Valid) Delay upon V_{DD2} Startup



Package Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	RH ≤ 50%, t = 1 minute; T_A = 25°C	5000	—	—	V_{rms}	a, b
Input-Output Resistance	R_{I-O}	V_{I-O} = 500 Vdc	10^{12}	10^{13}	—	Ω	b
		T_A = 100°C	10^{11}	—	—	Ω	b
Input-Output Capacitance	C_{I-O}	f = 1 MHz	—	1.4	—	pF	b
Input IC Junction-to-Ambient Thermal Resistance	θ_{JAI}	1 oz. trace, 2-layer PCB, still air, T_A = 25°C	—	83	—	°C/W	c
Output IC Junction-to- Ambient Thermal Resistance	θ_{JAO}	1 oz. trace, 2-layer PCB, still air, T_A = 25°C	—	85	—	°C/W	c

a. In accordance with UL 1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in the IEC/EN 60747-5-5 Insulation Characteristic table.

b. This is a two-terminal measurement: pins 1 to 8 are shorted together, and pins 9 to 16 are shorted together.

c. Maximum power dissipation in analog-side and digital-side ICs must be limited to ensure that their respective junction temperature is less than 125°C. The maximum permissible power dissipation is dependent on the thermal impedance and the ambient temperature.

Typical Performance Plots

Unless otherwise noted, T_A = 25°C, V_{DD1} = 5V, V_{DD2} = 3.3V, V_{IN+} = –50 mV to +50 mV, and V_{IN-} = 0V, f_{MCLKIN} = 20 MHz, with Sinc3 filter, 256 decimation ratio.

Figure 7: Offset vs. Temperature

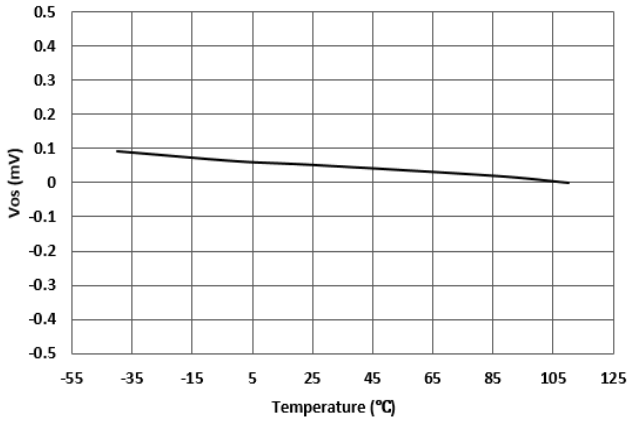


Figure 8: Offset vs. V_{DD1}

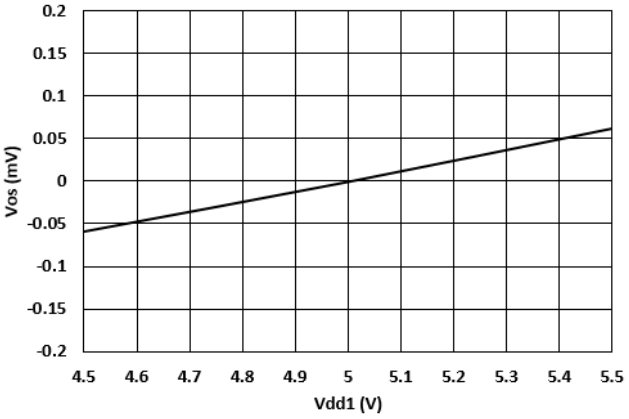


Figure 9: Offset vs f_{MCLKIN}

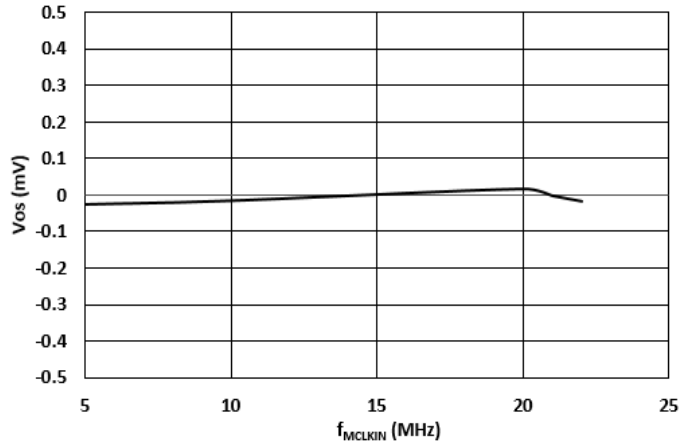


Figure 10: Gain Error vs. Temperature

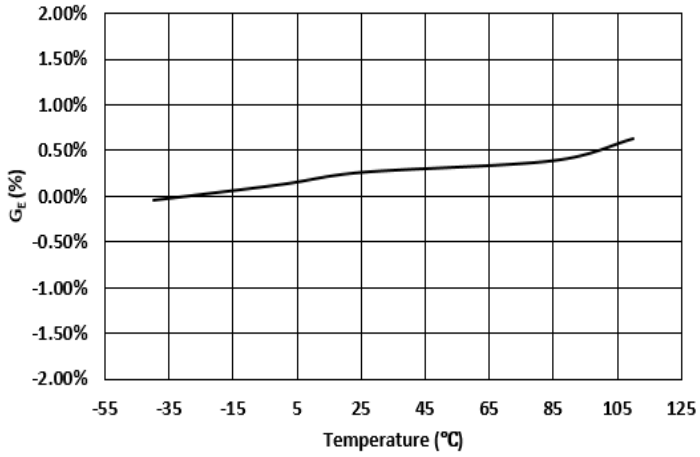


Figure 11: Gain Error vs f_{MCLKIN}

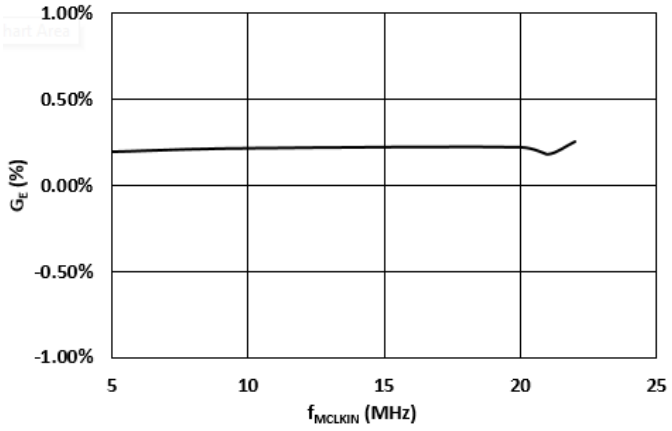


Figure 12: Gain Error vs V_{DD1}

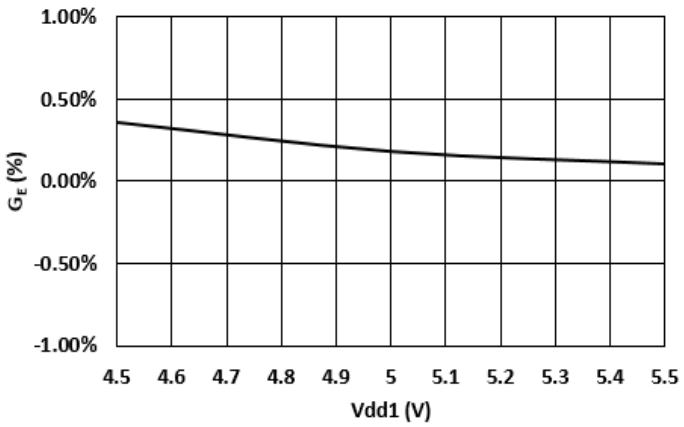


Figure 13: SNR vs. Temperature at Various f_{MCLKIN}

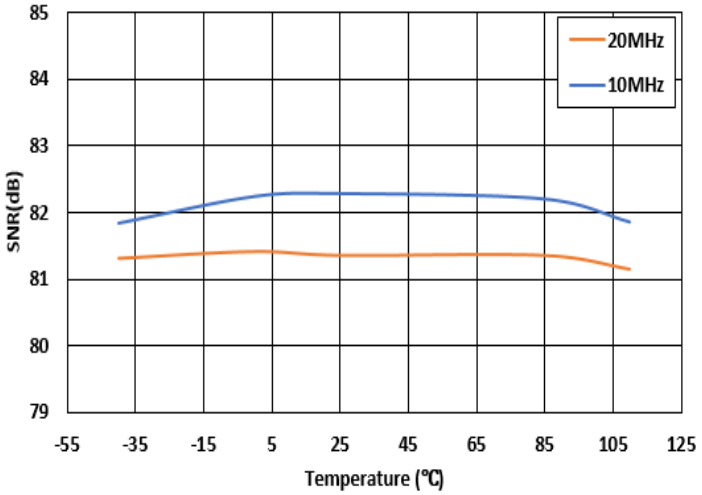


Figure 14: SNDR vs. Temperature at Various f_{MCLKIN}

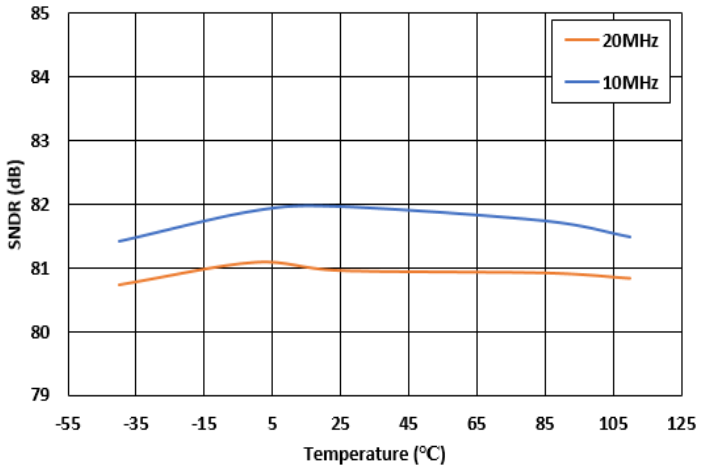


Figure 15: SNR vs. Input Voltage V_{IN}

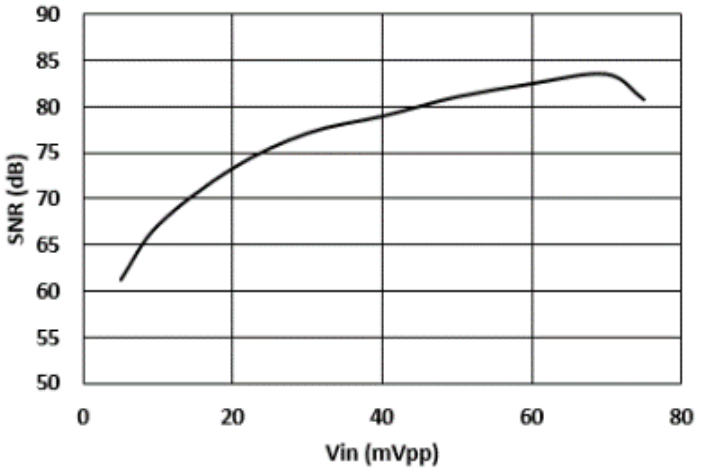


Figure 16: SNDR vs. Input Voltage V_{IN}

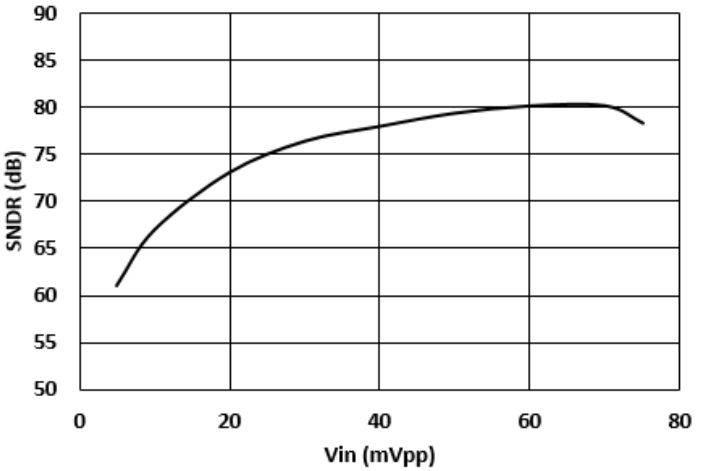


Figure 17: I_{DD1} vs. Input Voltage V_{IN} at Various f_{MCLKIN}

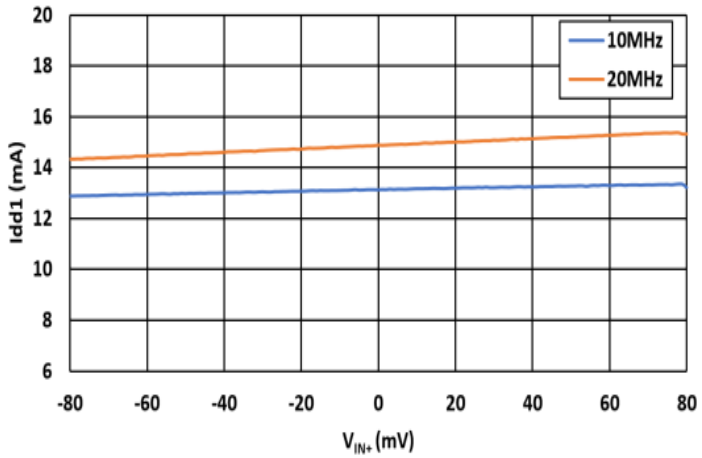


Figure 18: I_{DD1} vs. Temperature at V_{IN} = 0 mV

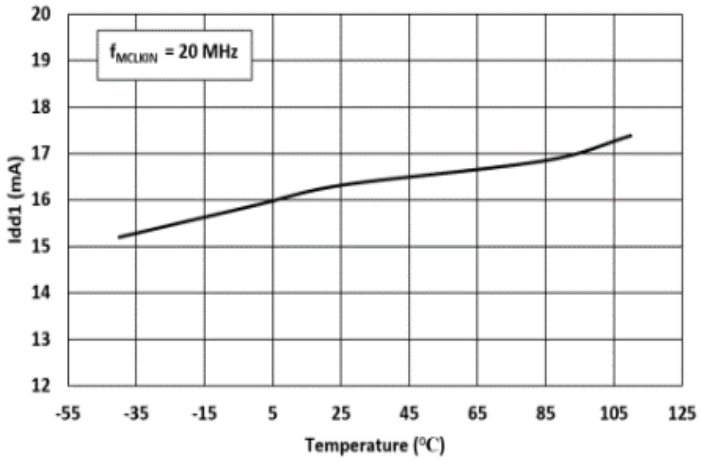


Figure 19: I_{DD2} vs. Input Voltage V_{IN} at Various f_{MCLKIN} and Various V_{DD2}

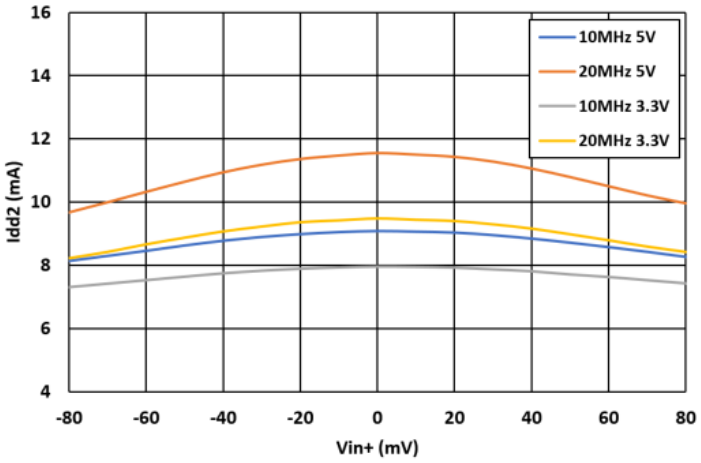


Figure 20: I_{DD2} vs Temperature at V_{IN} = 0 mV

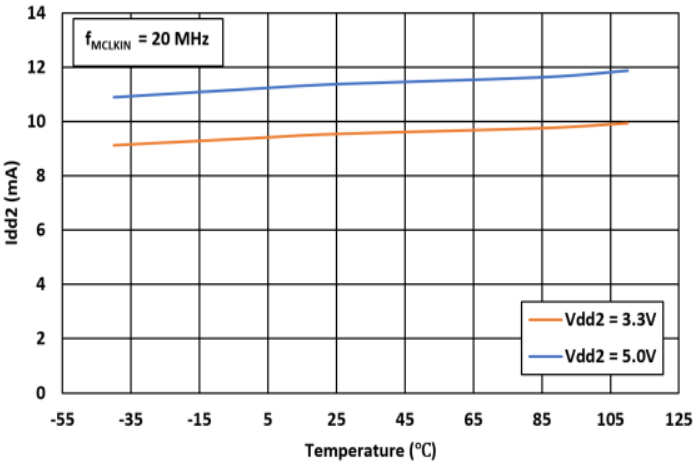
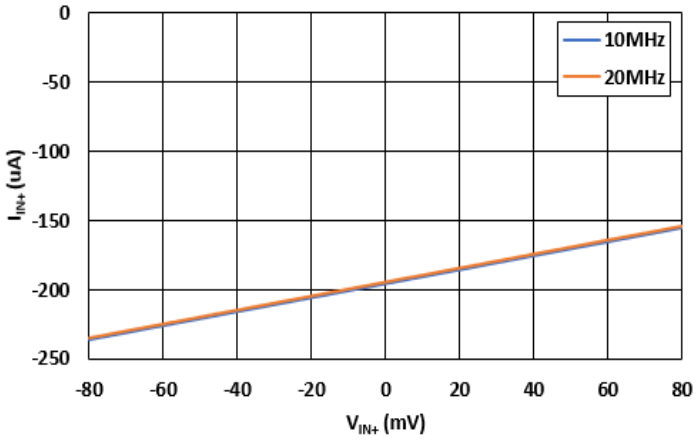


Figure 21: Input Current I_{IN} vs Input Voltage V_{IN} at Various f_{MCLKIN}



Definitions

Integral Nonlinearity (INL)

The INL is the maximum deviation of a transfer curve from a straight line passing through the endpoints of the ADC transfer function, with offset and gain errors adjusted out.

Differential Nonlinearity (DNL)

The DNL is the deviation of an actual code width from the ideal value of 1 LSB between any two adjacent codes in the ADC transfer curve. DNL is a critical specification in closed-loop applications. A DNL error of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

Offset Error

The offset error is the deviation of the actual input voltage corresponding to the mid-scale code (32,768 for a 16-bit system with an unsigned decimation filter) from 0V. The offset error can be corrected by software or hardware.

Gain Error

The gain error is the deviation of the actual V_{REF} from the ideal V_{REF} (80 mV). The actual V_{REF} is derived from the full-scale positive differential input voltage multiplied by the best fit-line gain. The best fit-line gain is the linear gain covering the entire linear-scale differential input range from –50 mV to 50 mV. The gain error can be corrected by software or hardware.

Actual V_{REF} = Full-Scale Positive Differential Input × Best Fit-Line Gain

$$Gain\ Error\ (\%) = [\frac{Actual\ VREF}{Ideal\ VREF}] - 1\ (\%)$$

Signal-to-Noise Ratio (SNR)

The SNR is the measured ratio of the AC signal power to the noise power below half of the sampling frequency. The noise power excludes harmonic signals and DC.

Signal-to-(Noise + Distortion) Ratio (SNDR)

The SNDR is the measured ratio of the AC signal power to the noise plus the distortion power at the output of the ADC. The signal power is the RMS amplitude of the fundamental input signal. The noise plus the distortion power is the RMS sum of all nonfundamental signals up to half the sampling frequency (excluding DC).

Effective Number of Bits (ENOB)

The ENOB determines the effective resolution of an ADC, expressed in bits, defined as follows:

ENOB = (SNDR – 1.76)/6.02

Isolation Transient Immunity (CMTI)

The isolation transient immunity specifies the minimum rate-of-rise/fall of a common-mode signal applied across the isolation boundary beyond which the modulator clock or data is corrupted.

Product Overview

Description

The ACPL-736J isolated sigma-delta (Σ-Δ) modulator converts an analog input signal into a high-speed (up to 21 MHz) single-bit data stream by means of a sigma-delta oversampling modulator. The time average of the modulator data is directly proportional to the input signal voltage. The modulator uses external clock ranges from 5 MHz to 21 MHz that are coupled across the isolation barrier. This arrangement allows synchronous operation of data acquisition to any digital controller and an adjustable clock for speed requirements of the application. The modulator data is encoded and transmitted across the isolation boundary where it is recovered and decoded into a high-speed data stream of digital ones and zeros. The original signal information is represented by the density of ones in the data output.

The other main function of the modulator (optocoupler) is to provide galvanic isolation between the analog signal input and the digital data output. It provides high noise margins and excellent immunity against isolation-mode transients that allow direct measurement of low-level signals in highly noisy environments, for example measuring motor phase currents in power inverters.

With a 0.5-mm minimum DTI, the ACPL-736J provides reliable double protection and high working insulation voltage, which is suitable for fail-safe designs. This outstanding isolation performance is superior to alternatives, including devices based on capacitive or magnetic coupling with DTI in the micro-meter range. Offered in an SO-16 package, the isolated ADC delivers the reliability, compact size, superior isolation, and overtemperature performance that motor drive designers need to accurately measure current, at a much lower price compared to traditional current transducers.

Analog Input

The ACPL-736J front-end contains a fully differential amplifier followed by a sigma-delta modulator. The fully differential analog inputs accept signals of ±50 mV (full scale ±80 mV), which is ideal for direction connection to shunt-based current sensing or other low-level signal sources applications such as motor phase current measurements.

Users can use a higher input range, for example ±75 mV (as long as it is within the full-scale range of ±80 mV), for the purpose of overcurrent or overload detection.

Latch-Up Consideration

The latch-up risk of CMOS devices needs careful consideration, especially in applications with a direct connection to the signal source that is subject to frequent transient noise. The well designed analog input structure of the ACPL-736J is resilient to transients, which are often encountered in highly noisy application environments such as motor drives and other power inverter systems. Other situations that can cause transient voltages to the inputs include short circuits and overload conditions. The ACPL-736J is tested to be able to reject a DC voltage of –2V and a 2-second transient voltage of –6V presented to the analog inputs without any latch-up or damage to the device.

Modulator Data Output

Input signal information is contained in the modulator output data stream, represented by the density of ones and zeros. The density of ones is proportional to the input signal voltage, as shown in Figure 22. A differential input signal of 0V ideally produces a data stream of ones 50% of the time and produces zeros 50% of the time. A differential input of –50 mV corresponds to a 18.75% density of ones, and a differential input of +50 mV is represented by a 81.25% density of ones in the data stream. A differential input of +80 mV or higher results in ideally all ones in the data stream, while an input of –80 mV or lower results in all zeros ideally. Table 3 shows this relationship.

Digital Filter

The original analog signal that is converted to a digital bit stream by the oversampling sigma-delta modulator can be recovered by means of filtering in the digital domain. A common and simple way is by implementing a cascaded integrated comb (CIC) filter or Sinc3 filter. The digital filter averages or decimates the oversampled bit stream and effectively converts it into a multibit digital equivalent code of the original analog input signal. With a 20-MHz external clock frequency, a 256 decimation ratio, and 16-bit word settings, the output data rate is 78 kHz (= 20 MHz/256). This filter can be implemented in an ASIC, an FPGA, or a DSP. Table 3 shows some of the equivalent digital codes with their corresponding input voltages.

Figure 22: Modulator Output vs. Analog Input

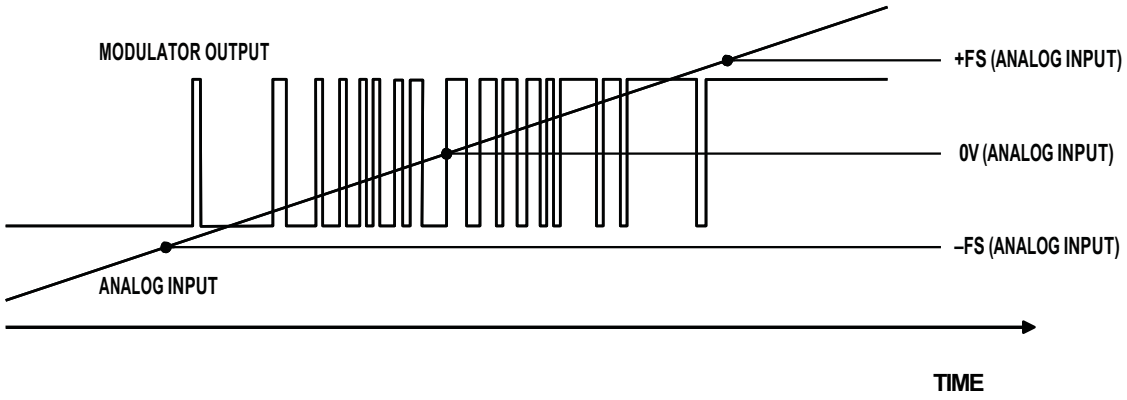


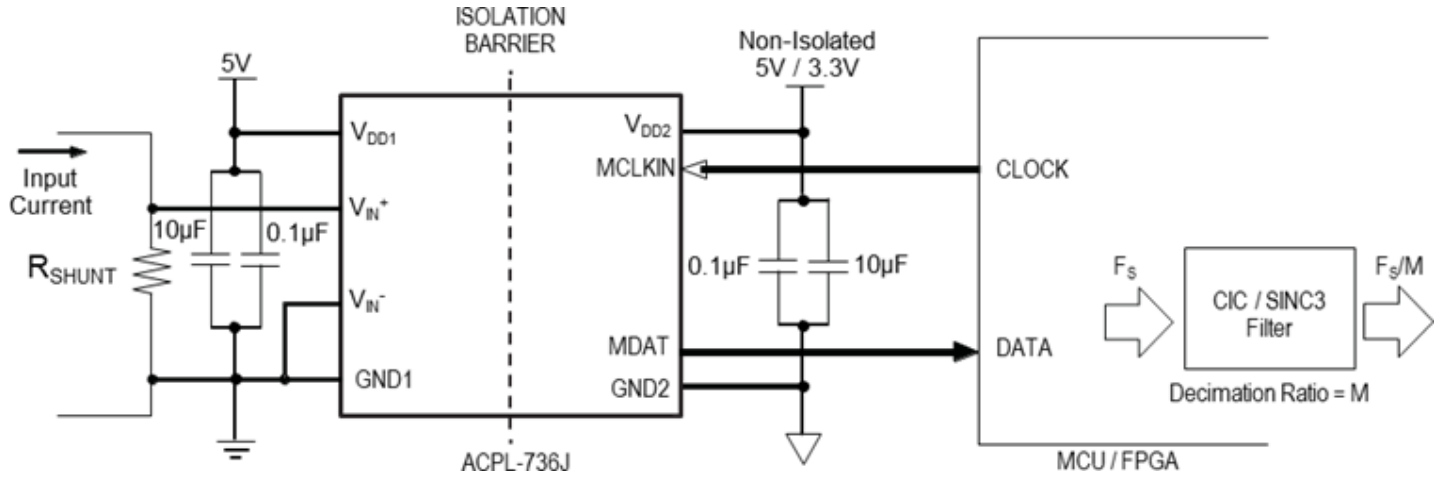
Table 3: Input Voltage with Ideal Corresponding Density of 1s at the Modulator Data Output and ADC Code[a, b]

Analog Input	Voltage Input	Density of 1s	ADC Code (16-Bit Unsigned Decimation)
Full-Scale Range	160 mV	—	—
+Full-Scale	+80 mV	100%	65,535
+Recommended Input Range	+50 mV	81.25%	53,248
Zero	0 mV	50%	32,768
–Recommended Input Range	–50 mV	18.75%	12,288
–Full-Scale	–80 mV	0%	0

a. With a bipolar offset binary coding scheme, the digital code begins with digital 0 at –FS input and increases proportionally to the analog input until the full-scale code is reached at the +FS input. The zero crossing occurs at the mid-scale input.

b. The ideal density of 1s at the modulator data output can be calculated by V_{IN}/160 mV + 50%; similarly, the ADC code can be calculated by (V_{IN}/160 mV) × 65,536 + 32,768, assuming a 16-bit unsigned decimation filter.

Figure 23: Typical Application Circuit with a Sinc3 Filter



NOTE: Parallel pairs of 10-µF and 0.1-µF bypass capacitors are recommended to be added and placed between pins V_{DD1} and GND1 and between pins V_{DD2} and GND2 of the ACPL-736J.

Application Information

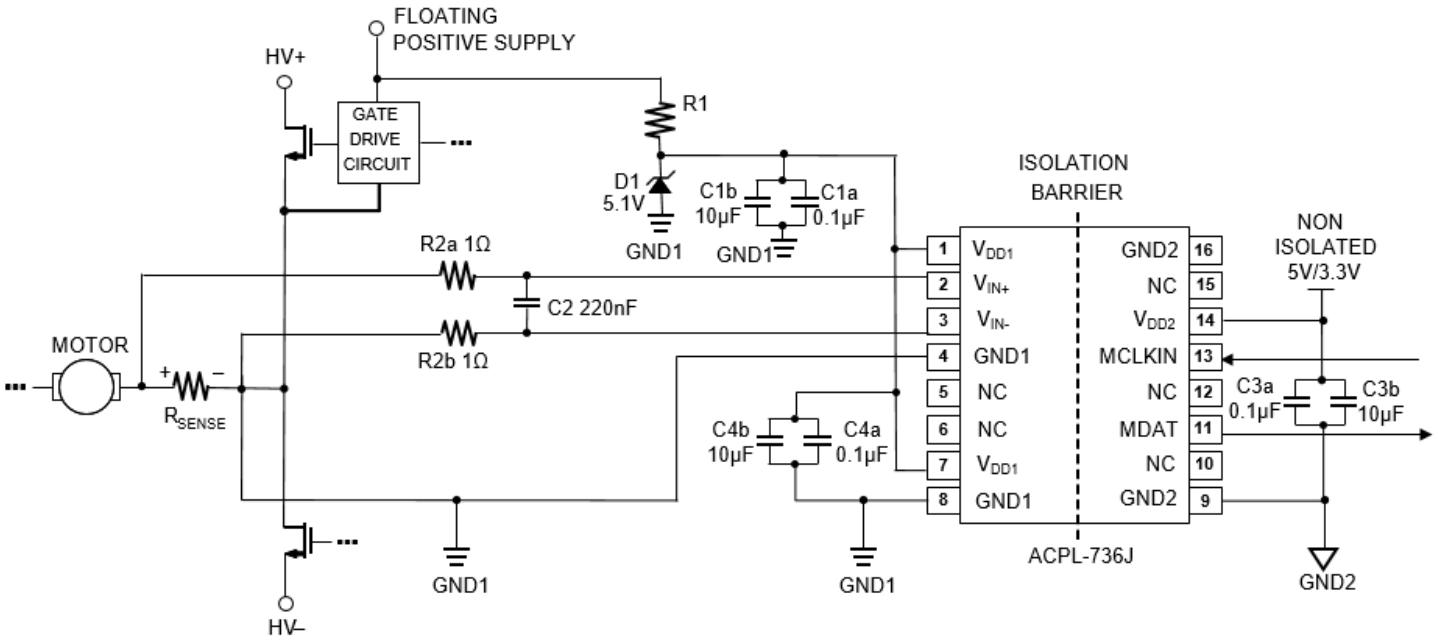
Digital Current-Sensing Circuit

Figure 24 shows a typical application circuit for motor control phase current sensing. By choosing the appropriate shunt resistance, any range of current can be monitored, from less than 1A to more than 300A.

Power Supplies and Bypassing

As shown in Figure 24, a floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5V using a low-cost, simple Zener diode configuration or a voltage regulator.

Figure 24: Typical Application Circuit for Motor Phase Current Sensing



The voltage from the current-sensing resistor or shunt (R_{SENSE}) is applied to the input of the ACPL-736J through an RCR anti-aliasing filter (R_{2a}, C_2, R_{2b}). Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance. The power supply for the isolated modulator is most often obtained from the same supply used to power the power transistor gate-drive circuit. If a dedicated supply is required, in many cases it is possible to add an additional winding on an existing transformer. Otherwise, some sort of simple isolated supply can be used, such as a line powered transformer or a high-frequency DC-DC converter.

To help attenuate high-frequency power-supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor. A ferrite bead is also recommended to be placed near the V_{DD1} pin to filter out any high-frequency noise in the supply. As shown in Figure 24, bypass capacitors (C_{1a}, C_{1b}, C_{3a} to C_{3b}) should be located as close as possible to the input and output power-supply pins of the isolated modulator. The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolated modulator.

Tantalum and ceramic capacitors are also recommended over electrolytic capacitors due to their lower ESR, which translates to a faster response to support the switching currents required by the isolated modulator. A 100-nF bypass capacitor (C_2) is also recommended at the input due to the switched-capacitor nature of the input circuit. The input bypass capacitor, together with the R_2 resistors, also forms part of the anti-aliasing filter, which is recommended to prevent high-frequency noise from aliasing down to lower frequencies and interfering with the input signal.

Figure 24 shows the recommended method for connecting the isolated modulator to the shunt resistor. V_{IN+} and V_{IN-} of the ACVPL-736J are connected directly across the shunt resistor with two conductors, and GND1 is connected to the shunt resistor with a third conductor for the power-supply return path. The power-supply return path functions as the sense line to the negative terminal of the current shunt. By referencing the input circuit to the negative side of the sense resistor, any load-current-induced noise transients on the shunt are seen as a common-mode signal and do not interfere with the current-sense signal. This is important because the large load currents flowing through the motor drive, along with the parasitic inductances inherent in the wiring of the circuit, can generate both noise spikes and offsets that are relatively large compared to the small voltages that are being measured across the current shunt.

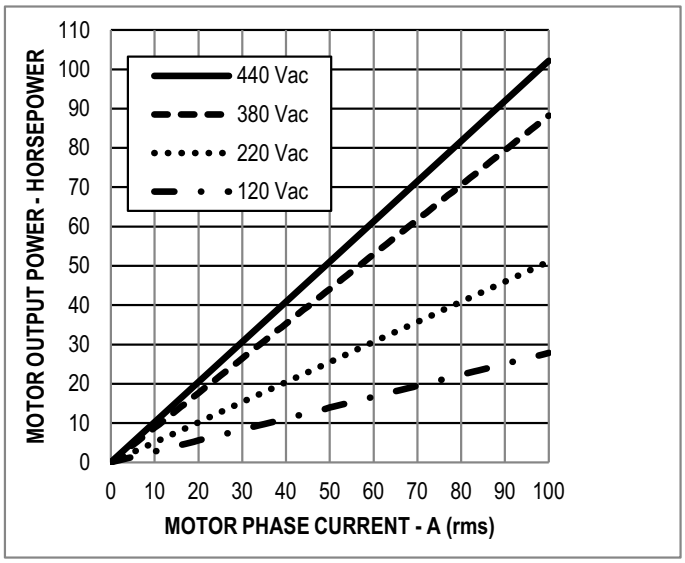
In some applications, however, supply currents flowing through the power-supply return path may cause offset or noise problems. The input currents induced by the common-mode of the fully differential amplifier on both of the pins are balanced on the filter resistors, R_{2a} and R_{2b}, and cancel each other out. Any noise induced on one pin is coupled to the other pin by the capacitor C_2 and creates only common mode noise, which is rejected by the device. When connected this way, both input pins should be bypassed. To minimize electromagnetic interference of the sense signal, all conductors that connect the isolated modulator to the sense resistor should be either twisted pair wire or closely spaced traces on a PC board.

If the same power supply is used for both the gate-drive circuit and the current-sensing circuit, it is very important that the connection from GND1 of the isolated modulator to the sense resistor be the only return path for the supply current to the gate-drive power supply in order to eliminate potential ground loop problems. The only direct connection between the isolated-modulator circuit and the gate-drive circuit should be the positive power supply line.

Shunt Resistors

The current-sensing shunt resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt-induced voltage spikes that could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). Choosing a particular value for the shunt is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller shunt resistances decrease power dissipation, whereas larger shunt resistances can improve circuit accuracy by utilizing the full input range of the isolated modulator.

Figure 25: Motor Output Horsepower vs. Motor Phase Current and Supply



The first step in selecting a shunt is determining how much current the shunt will be sensing. Figure 25 shows the RMS current in each phase of a three-phase induction motor as a function of average motor output power (in horsepower, hp) and motor drive supply voltage. The maximum value of the shunt is determined by the current being measured and the maximum recommended input voltage of the isolated modulator. The maximum shunt resistance can be calculated by taking the maximum recommended input voltage and dividing by the peak current that the shunt should see during normal operation. For example, if a motor has a maximum RMS current of 70 A_{rms} and can experience up to 50% overloads during normal operation, then the peak current is 150A (= 70 × 1.414 × 1.5). Assuming a maximum input voltage of 50 mV without overload conditions, the

maximum value of shunt resistance in this case would be about 0.5 mΩ. Under overload conditions, the maximum input voltage is 75 mV (150A × 0.5 mΩ), well within the ±80-mV FSR.

The maximum average power dissipation in the shunt can also be easily calculated by multiplying the shunt resistance times the square of the maximum RMS current, which is about 2.45W in the previous example.

If the power dissipation in the shunt is too high, the resistance of the shunt can be decreased below the maximum value to decrease power dissipation. The minimum value of the shunt is limited by the precision and accuracy requirements of the design. As the shunt value is reduced, the output voltage across the shunt is also reduced, which means that the offset and noise, which are fixed, become a larger percentage of the signal amplitude. The selected value of the shunt will fall somewhere between the minimum and maximum values, depending on the particular requirements of a specific design.

When sensing currents large enough to cause significant heating of the shunt, the temperature coefficient (tempco) of the shunt can introduce nonlinearity due to the signal-dependent temperature rise of the shunt. The effect increases as the shunt-to-ambient thermal resistance increases. This effect can be minimized either by reducing the thermal resistance of the shunt or by using a shunt with a lower tempco. Lowering the thermal resistance can be accomplished by repositioning the shunt on the PC board, by using larger PC board traces to carry away more heat, or by using a heat sink.

For a two-terminal shunt, as the value of shunt resistance decreases, the resistance of the leads becomes a significant percentage of the total shunt resistance. This has two primary effects on shunt accuracy. First, the effective resistance of the shunt can become dependent on factors such as how long the leads are, how they are bent, how far they are inserted into the board, and how far solder wicks up the lead during assembly (these issues will be discussed in more detail shortly). Secondly, the leads are typically made from a material such as copper, which has a much higher tempco than the material from which the resistive element itself is made, resulting in a higher tempco for the shunt overall. Both of these effects are eliminated when a four-terminal shunt is used. A four-terminal shunt has two additional terminals that are Kelvin-connected directly across the resistive element itself; these two terminals are used to monitor the voltage across the resistive element, whereas the other two terminals are used to carry the load current. Because of the Kelvin connection, any voltage drops across the leads carrying the load current should have no impact on the measured voltage.

Table 4 shows examples of several two-terminal and four-terminal surface-mount type shunt resistors from various suppliers suitable for sensing currents in motor drives up to 70 A_{rms} (71 hp or 53 kW).

Table 4: Example of Two-Terminal and Four-Terminal Shunt Resistors for Motor Drives up to 70 A_{rms}

Manufacturer/Shunt Resistor Part Number	Shunt Resistor Type	Shunt Resistance	Maximum RMS Current	Motor Power Range 120 Vac to 440 Vac	
		mΩ	A	hp	kW
KOA/CSR series	Four-terminal	5	7	1.8–6.7	1.4–5
Isabellenhütte/BVS series	Two-terminal				
Vishay/WSL4026 series	Four-terminal	2	17	4–17	3–13
Isabellenhütte/BVE series	Two-terminal				
KOA/PSG4 series	Four-terminal	1	35	9–36	7–27
KOA/PSB series	Two-terminal				
Isabellenhütte/BVR series	Four-terminal	0.5	70	19–72	14–54
KOA/PSJ2 series	Two-terminal				

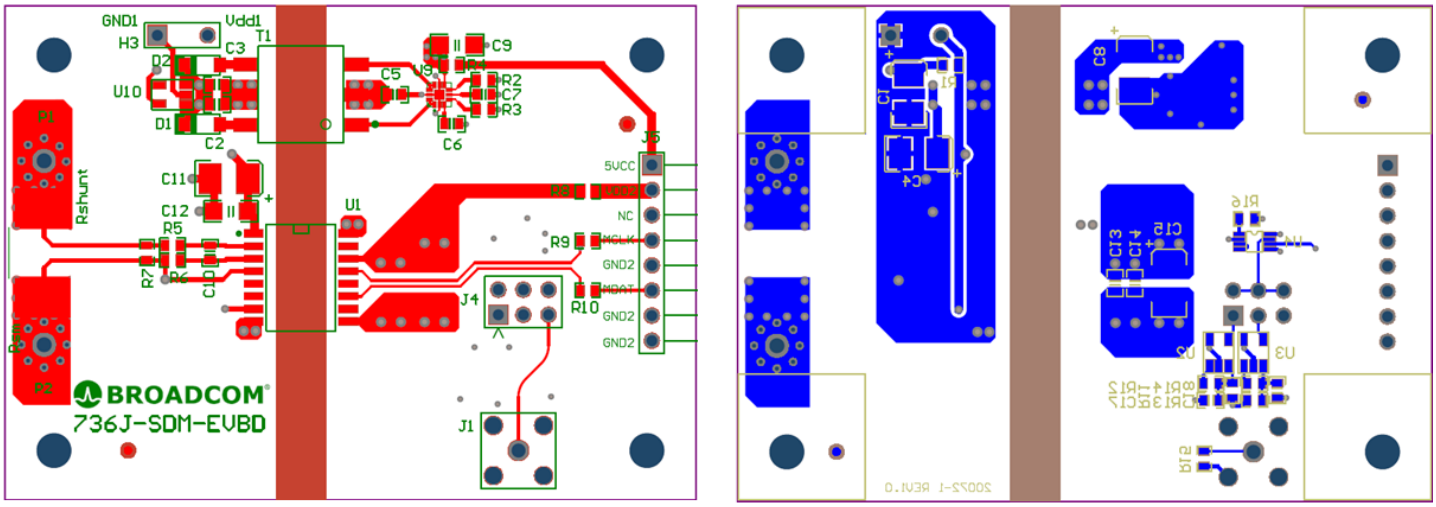
When laying out a PC board for the shunts, a couple of points should be kept in mind. The Kelvin connections to the shunt should be brought together under the body of the shunt and then run very close to each other to the input of the isolated modulator; this minimizes the loop area of the connection and reduces the possibility of stray magnetic fields interfering with the measured signal. If the shunt is not located on the same PC board as the isolated modulator circuit, a tightly twisted pair of wires can achieve the same result.

Also, multiple layers of the PC board can be used to increase current carrying capacity. Numerous plated-through vias should surround each non-Kelvin terminal of the shunt to help distribute the current between the layers of the PC board. The PC board should use 2-oz. or 4-oz. copper for the layers, resulting in a current carrying capacity in excess of 20A. Making the current-carrying traces on the PC board fairly large can also improve the shunt's power dissipation capability by acting as a heat sink. Liberal use of vias where the load current enters and exits the PC board is also recommended.

PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, and the use of ground and power planes. Figure 26 shows an example of PCB layout where the V_{DD1} is supplied from an isolated 5V/5V push-pull dc-dc converter. The input anti-aliasing filter network should be placed as close as possible to the input pin to minimize any stray inductance. The layout of the PCB can also affect the isolation transient immunity (CMR) of the isolated modulator, due primarily to stray capacitive coupling between the input and output circuits. To obtain optimal CMR performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the isolated modulator.

Figure 26: Example of Good PCB Layout for the ACPL-736J (CMOS Output)



Top Layer

Bottom Layer