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# AND8273/D

# Design of a 100 W Active Clamp Forward DC-DC Converter for Telecom Systems Using the NCP1562

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APPLICATION NOTE

## INTRODUCTION

The NCP1562 PWM controller contains all the features and flexibility needed to implement an active clamp forward dc−dc converter. This IC operates from an input supply up to 150 V, thus covering the input voltages usually found in telecom, datacom and 42 V automotive systems. One can also note that the NCP1562 can be used in mains related applications (e.g. desktop, server, flat TVs) as it can be supplied by an auxiliary power supply.

The NCP1562 is the ideal choice for new generation isolated fixed switching frequency dc−dc converters using the active clamp topology with synchronous rectification to achieve extremely high conversion efficiency. This controller will help designers cope with their daily challenge, “small form factor highly protected module” through the following features:

- **Dual Outputs with Adjustable Overlap Delay:** provide design flexibility. Output 1 (OUT1) drives the main switch in a forward or flyback converter topology. Output 2 (OUT2) can be used to drive an active clamp/reset switch, a synchronous rectifier switch, or both. OUT2 has an adjustable overlap delay to prevent simultaneous conduction of the switching elements.
- **Soft−Stop:** discharges the active clamp capacitor prior to turn off to eliminate unwanted oscillations.
- **An Internal Startup Regulator:** provides power to the NCP1562 during startup. Once the system powers up, the regulator is disabled, thus reducing power consumption. The regulator can be powered directly from the input line.
- **Soft−Start:** allows the system to turn on in a controlled manner and reduce stress on system components.
- **Adjustable Maximum Duty Ratio:** allows the design to be optimized without a penalty on drain voltage. Duty ratio is controlled within ±5%.
- **Adjustable Volt−second Limit:** prevents transformer saturation and improve transient response.
- **Line Feedforward:** adjusts the duty ratio inversely proportional to line voltage, allowing the controller to respond in the same cycle to line voltage changes. It provides the controller some advantages of current−mode control, while eliminating noise susceptibility, low power jitter and the need for ramp compensation.
- **Dual Mode Overcurrent Protection Circuit:** handles momentary and continuous overcurrent conditions differently to provide the best tradeoff in system performance and safety.
- **Line Under/Overvoltage Detector:** circuits enable the device when the line voltage is within the pre−selected voltage range. A resistor divider from the input line biases the under and overvoltage detectors. The accurate UV limit allows the converter to operate at high duty ratio without creating additional component stresses.

## DESIGN SPECIFICATIONS

The flexibility of the NCP1562 is demonstrated by examining a detailed design of a dc−dc converter for the telecom system. The converter delivers up to 100 W at 3.3 V. The converter specifications are listed in Table 1. A forward active clamp topology is selected for the converter, as it provides very high efficiency.

**Table 1. Design Specifications**

| Parameter | Symbol | Min | Max |
|---|---|---|---|
| Input Voltage | $V_{in}$ (V) | 33 | 76 |
| Frequency | $f_{SW}$(kHz) | 350 (typ) | |
| Full Load Efficiency | η (%) | 90 | – |
| Duty Ratio | D | | 65% |
| Output Voltage | $V_{out}$ (V) | 3.267 | 3.333 |
| Output Voltage Ripple | $V_{out(rip)}$ (mV) | | 50 |
| Output Current | $I_{out}$ (A) | 3 | 30 |
| Output Power | $P_{out}$ (W) | – | 100 |
| Ambient Temperature | $T_A$ (C) | | 50 |
| Derating Factor | – | 90% | |

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## ACTIVE CLAMP FORWARD TOPOLOGY

The active clamp forward (ACF) topology has multiple advantages compared to a traditional forward converter. The benefits of the active clamp topology can be easily maximized once the unique characteristics of this topology are fully understood. Figure 1 shows a simplified schematic of an active clamp forward topology. The transformer model (TX1) consists of an ideal transformer, magnetizing ($L_{MAG}$) and leakage ($L_{LKG}$) inductances.

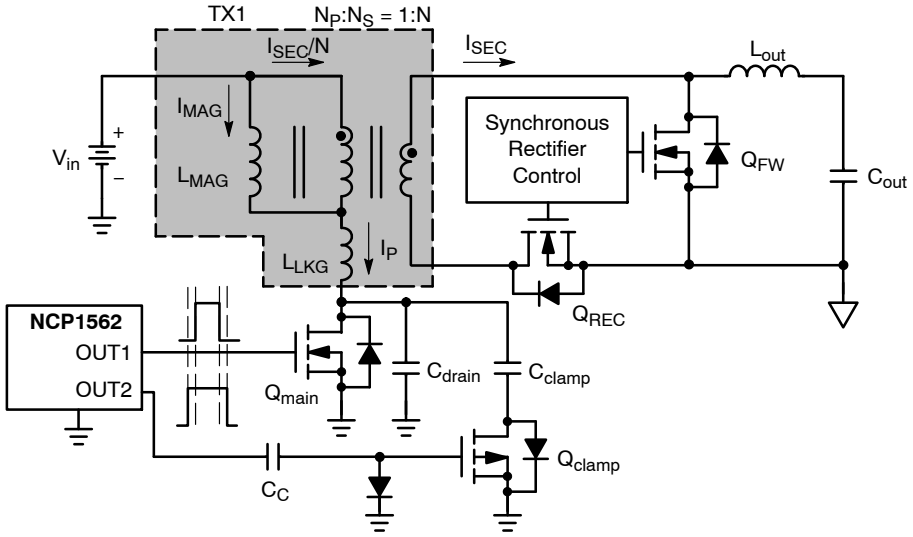


**Figure 1. Active Clamp Forward Converter**

The active clamp network consists of the P−channel clamp switch ($Q_{clamp}$) and clamp capacitor ($C_{clamp}$). This configuration is known as low side active clamp. A high side clamp could have been implemented using an N−channel MOSFET and clamp capacitor in parallel with the transformer primary. However, it requires a floating gate drive signal increasing system cost and complexity.

The differences between traditional and active clamp forward converters are during the main switch off time. In the active clamp topology, the transformer is reset at a lower voltage during the complete off time instead of a higher voltage during a shorter period of time. Figure 2 shows a comparison between the drain waveforms of both topologies. The traditional forward waveform was taken with a primary:reset winding ratio of 5:3 instead of 1:1. The 5:3 ratio allowed operation above 50% duty cycle.

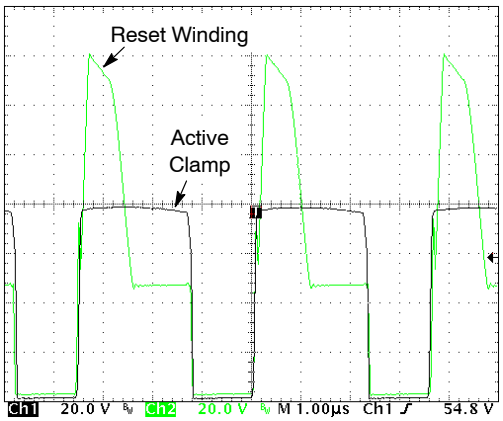


**Figure 2. Drain Voltage Waveforms for Traditional and Active Clamp Forward Topologies**

The differences go beyond the replacement of the reset winding and catch diode with a clamp capacitor and a clamp switch. There are many system considerations and benefits provided by the active clamp topology as described below:

1. Facilitates zero volt switching (ZVS) or low−voltage/soft switching of the main and active clamp switches.
2. The ability to operate above 50% duty ratio with a high turns ratio without a penalty on drain voltage.
3. A high turns ratio reduces:
   a.) The reflected output current component on the primary side allowing the use of a smaller $Q_{main}$.
   b.) The secondary voltage allowing the use of lower voltage rectification elements.
4. Lower output inductance is required due to the higher duty ratio.
5. Signals for driving a synchronous rectifier are readily available.

The operation of the active clamp forward is discussed in detail with the use of Figure 3. This figure shows the power stage waveforms of an active clamp forward converter in steady state. One switch cycle is divided in several time intervals to facilitate the analysis.

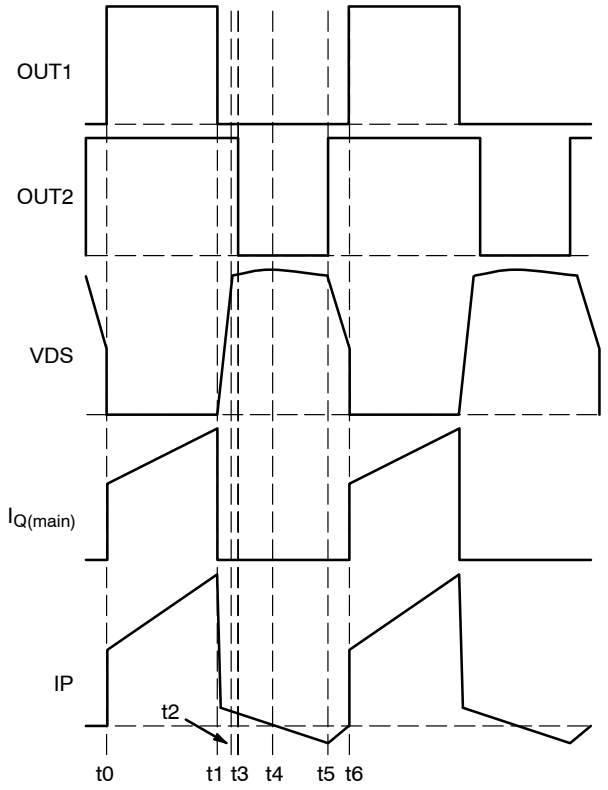


**Figure 3. Active Clamp Forward Waveforms**

Time interval t0 – t1:

The main switch turns on at t0. The active clamp switch remains off. The primary current ($I_P$) flows through the transformer and the main switch. This current is the sum of the transformer magnetizing ($I_{MAG}$) and reflected secondary currents. No current flows through $Q_{clamp}$ and current flows in the secondary side through the forward rectifier, $Q_{REC}$. The primary current continues to build while $Q_{main}$ is on.

Time interval t1 – t2:

The main switch turns off at t1. The forward rectifier turns off at t1 eliminating the reflected secondary current component from $I_P$ if the leakage inductance effect is neglected. The primary current is now the magnetizing current. It continues to flow in the same direction charging the drain capacitance, $C_{drain}$.

Time interval t2 – t3:

At time t2 the drain voltage reaches the clamp capacitor voltage. The primary current charges both the drain capacitance and $C_{clamp}$. The primary current flows through the body diode of $Q_{clamp}$. The clamp capacitor is several orders of magnitude larger $C_{drain}$, causing the voltage slope to drop. The drain ripple voltage is determined by the resonance between $L_{MAG}$ and $C_{clamp}$.

Time interval t3−t4:

The active clamp switch can turn on at any time between t2 and t4 under ZVS conditions. Once $Q_{clamp}$ turns on, current flows through its channel. The magnitude of $I_P$ is decreasing and reaches zero at t4. It is imperative for $Q_{clamp}$ to be on at t4. Otherwise, $I_P$ will not have a path to reverse its direction.

Time interval t4−t5:

The primary current has reversed direction and is now discharging $C_{clamp}$. The drain voltage begins to decrease. The magnetizing current continues to build up in the reverse direction.

Time interval t5−t6:

The active clamp switch turns off at t5. It is critical to achieve a fast turn off $Q_{clamp}$ to force the magnetizing current to discharge the drain capacitance. Otherwise, current will continue flowing through $Q_{clamp}$.

The drain voltage decays as the drain capacitance is discharged. The minimum drain voltage is determined by the inductive energy ($E_L$) stored in the magnetizing and leakage inductances. If the inductive energy is greater than the capacitive energy stored in the drain capacitance, ZVS is achieved. If the magnetizing energy is not enough, an external inductor can be added to facilitate ZVS.

The inductive energy is increased by reducing $L_{MAG}$. This might be counter intuitive. But let me explain; Let's start with the magnetizing energy equation given by Equation 1.

$$E_{L(MAG)} = \frac{1}{2} \cdot L_{MAG} \cdot I_{MAG}^2 \qquad \text{(eq. 1)}$$

For a given voltage and on time, the $L_{MAG}$ and $I_{MAG}$ product is constant. That is, if $L_{MAG}$ decreases by $^1/_2$, $I_{MAG}$ increases by 2. As $I_{MAG}$ is squared, the net effect is an increase in energy.

## DESIGN PROCEDURE

The converter design is divided in several steps to ease the design process. The process begins with the power stage as it determines most of the system components. The design continues with the feedback loop followed by the setup of the controller, the NCP1562. Finally, the system performance is evaluated and compared to the design target.

Throughout this application note, operation at the minimum and maximum input voltages are referred as low and high line, respectively.

## TRANSFORMER

A power transformer (TX1) is used to step down the voltage and provide voltage isolation between the input supply and the load. The transformer in this design has three windings; primary, secondary and auxiliary.

Contrary to a traditional forward transformer, an active clamp transformer is designed with low magnetizing inductance. The stored magnetizing energy is used to discharge the drain capacitance and facilitate ZVS as explained earlier. In addition, $L_{MAG}$ affects the loop response as it affects a pair of complex zeros introduced by the active clamp stage. It is discussed later in the feedback loop section.

The input to output voltage relationship is described by Equation 2.

$$V_{out} = \left(\frac{V_{in} - V_{DS(on)}}{N} - V_f\,(QREC)\right) \cdot D \quad \text{(eq. 2)}$$

where, N is the primary to secondary turns ratio, $V_{DS(on)}$ is the voltage drop across $Q_{main}$, $V_{f(QREC)}$ is the voltage drop across $Q_{REC}$, D is the duty ratio and $V_{in}$ is the input voltage. Equation 2) is used to select N given a target maximum duty ratio. An additional factor to consider in the selection of N is the drain voltage of the main switch ($V_{DS}$) during the off time as it depends on the duty ratio. Equation 3 shows the relationship between $V_{DS}$ and D.

$$V_{DS} = \frac{V_{in}}{1 - D} \quad \text{(eq. 3)}$$

The NCP1562 Excel−based design tool (downloadable from http://www.onsemi.com). provides an easy way to evaluate the interaction between the turns ratio, duty ratio and maximum drain voltage as shown in Figure 4. The drain voltage is almost constant over the complete operating range. A high turns ratio is desired to reduce the primary current and the secondary voltage. However, it causes the drain voltage to increase very rapidly at low line. The ideal turns ratio is the one that achieves equal drain voltages at low and high line.

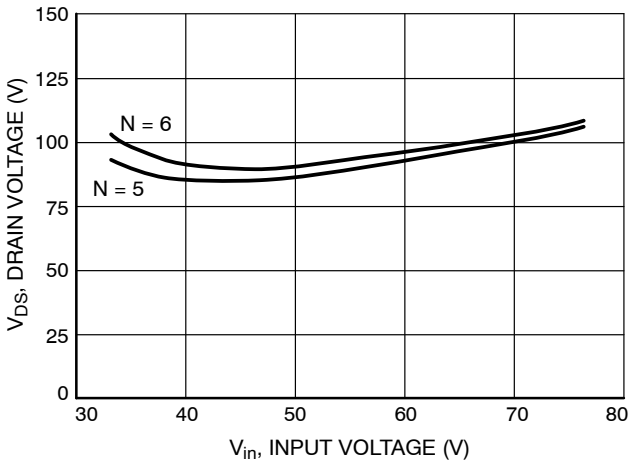


**Figure 4. Clamp Voltage vs. Input Voltage for Several Turns Ratios**

Using the design tool a turns ratio of 6 is selected for a maximum duty ratio of 63%. The ideal turns ratio is 6.5, but it would have increased the complexity of the transformer. In high current output converters, it is desired to keep the secondary turns at the lowest level (e.g. 1 turn) to reduce conduction losses. The primary turns ($N_P$) are set at 6 and the secondary turns ($N_S$) are set at 1. A 12:2 ($N_P$:$N_S$) ratio could have been used to reduce core losses. Low core losses are beneficial when conduction losses are low, as can be the case when operation at high line. The magnetizing inductance is set at 120 μH to reduce conduction losses.

A planar transformer is selected due to its low profile and repeatable characteristics. The custom transformer is manufactured by Payton Planar Magnetics and can be easily ordered under part number 51665.

## ACTIVE CLAMP STAGE

The active clamp topology recycles the transformer magnetizing energy using a resonant circuit. This resonant circuit is composed of the magnetizing inductance and clamp capacitor. The parasitic drain capacitance and leakage inductance are ignored as they are very small. The resonant frequency of $L_{MAG}$ and $C_{clamp}$ is selected low enough to maintain a constant voltage during the main switch off time. That is, the resonant period is significantly larger than the switching period of the controller.

The clamp capacitor determines the drain ripple voltage ($V_{DS(ripple)}$) during the main switch off time. The ripple voltage is inversely proportional to $C_{clamp}$. The active clamp capacitor also affects the loop response as it contributes to a pair of complex zeros introduced by the active clamp stage. It is discussed later in the Feedback Loop Section. If duty ratio changes rapidly, the voltage across $C_{clamp}$ has to change accordingly. Otherwise, the transformer may saturate. Therefore, a tradeoff between ripple voltage and transient response has to be considered in the selection of $C_{clamp}$. The design tool facilitates the selection of $C_{clamp}$ by plotting $V_{DS(ripple)}$ and the normalized peak flux excursion vs $C_{clamp}$ as shown in Figure 5.

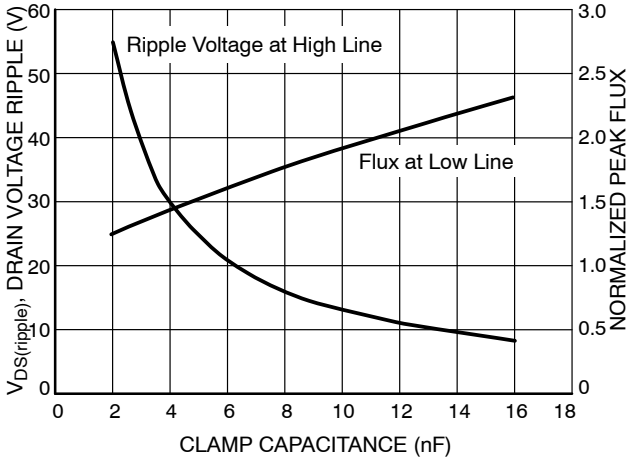


**Figure 5. $V_{DS(ripple)}$ and Normalized Peak Flux vs. $C_{clamp}$**

The magnetizing current charges and discharges the active clamp capacitor every cycle and is given by Equation 4.

$$I_{MAG} \approx \frac{V_{in} \cdot D}{f_{SW} \cdot L_{MAG}} \quad \text{(eq. 4)}$$

It is absolutely critical to consider the ripple current rating in the selection of $C_{clamp}$. Otherwise, the capacitor may overheat. The minimum ripple current rating of $C_{clamp}$ is determined by the magnetizing rms current. Assuming the magnetizing current reverses direction halfway during the off time, the clamp capacitor rms current is approximated by Equation 5.

$$I_{Cclamp(rms)} \approx \frac{V_{in} \cdot D}{f_{SW} \cdot L_{MAG}} \sqrt{\frac{1 - D}{2}} \quad \text{(eq. 5)}$$

The worst case condition is at high line.

Using the Design Tool, an rms magnetizing current of 0.294 A is calculated. A ceramic capacitor is preferred due its low equivalent series resistance (ESR). TDK's C3216X7R2J103M is used. Although maximum drain voltage of this design is 150 V, a 630 V capacitor is used as it is readily available.

### OUTPUT L−C FILTER

The output L−C ($L_{out}$−$C_{out}$) filter averages the square wave signal at the transformer output. The output inductor, $L_{out}$, is sized such that it operates in continuous conduction mode at the minimum output current, $I_{out(min)}$ using Equation 6.

$$L_{out} = \frac{V_{out} \cdot \left(\frac{1 - D_{(min)}}{f_{SW}}\right)}{2 \cdot I_{out(min)}} \quad \text{(eq. 6)}$$

where, $D_{(min)}$ is the minimum duty ratio. Solving Equation 6,

$$L_{out} = \frac{3.3 \cdot \left(\frac{1 - 0.271}{350}\right)}{2 \cdot 3} = 1.15\ \mu H$$

using the $D_{(min)}$ provided by the Design Tool, a minimum inductance of 1.15 μH is required. A custom 1.5 μH inductor from Payton Planar Magnetics is used. It can be easily ordered under part number 51666.

The inductor ripple current, $I_{out(rip)}$, reaches its maximum value at high line and it is given by Equation 7.

$$I_{out(rip)} = \frac{V_{out} \cdot \frac{1 - t_{on(min)}}{f_{SW}}}{L_{out}} \quad \text{(eq. 7)}$$

Solving Equation 7,

$$I_{out(rip)} = \frac{3.3 \cdot \left(\frac{1 - 0.271}{350}\right)}{1.5} = 4.58\ A$$

a maximum ripple current of 4.58 A is obtained. Figure 6 shows the inductor current at low and high line as provided by the Design Tool.

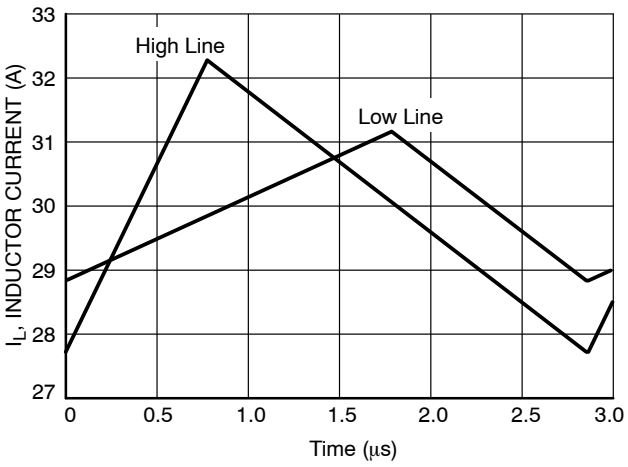


**Figure 6. Calculated Output Inductor Current at Low and High Conditions**

The minimum output capacitance required to maintain the output voltage ripple below our target of 50 mV is calculated using Equation 8.

$$C_{out} = \frac{I_{out(rip)}}{8 \cdot f_{SW} \cdot V_{out(rip)}} \quad \text{(eq. 8)}$$

A minimum capacitance of 33 μF is required. The capacitor ESR also affects the output voltage ripple as shown in Equation 9.

$$V_{out(rip)} = I_{out(rip)} \cdot R_{ESR} \quad \text{(eq. 9)}$$

In order to maintain $V_{out(rip)}$ below our target, $R_{ESR}$ has to be below 10.9 mΩ.

Please consider that Equation 8 provides a minimum value to maintain $V_{out(rip)}$ within target. In most cases, a higher $C_{out}$ is required to meet voltage holdup requirements and shape the frequency response of the converter as it is described later in the Feedback Loop Section. For this design, $C_{out}$ is set at 544 μF using a parallel combination of tantalum capacitors for bulk capacitance and ceramic capacitors for $R_{ESR}$ reduction.

### MAIN SWITCH

A MOSFET is used as the main switch. Several factors, including current, voltage stress and power dissipation are considered for the MOSFET selection.

The shape of the primary current is shown in Figure 7. It consists of the primary magnetizing and reflected output currents. The valley of the primary current, $I_{P(VL)}$ is approximated to the inductor current divided by the turns ratio.

In practice, $I_{P(VL)}$ is slightly less as the magnetizing current starts negative due to the resonant transition. But it is a good approximation as the magnetizing current is significantly smaller than the reflected output inductor current.

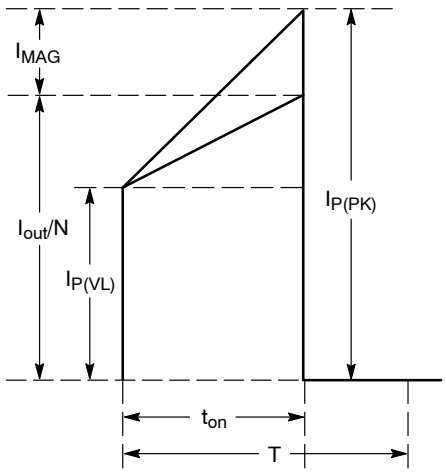


**Figure 7. Primary Current Waveform**

The primary peak current, $I_{P(PK)}$, is given by Equation 10. The maximum $I_{P(PK)}$ occurs at high line when the output inductor ripple current is at its highest.

$$I_{P(PK)} = \frac{I_{out} + \frac{I_{out(rip)}}{2}}{N} + \frac{V_{in} \cdot D}{L_{MAG} \cdot f_{SW}} \quad \text{(eq. 10)}$$

The main switch experiences conduction and switching losses. The conduction losses are given by Equation 11.

$$P_{con} = I_{P(rms)}^2 \cdot R_{DS(on)} \quad \text{(eq. 11)}$$

where, $R_{DS(on)}$ is the switch on resistance and $I_{P(rms)}$ is the primary rms current. The primary rms current is given by Equation 12.

$$I_{P(RMS)} = \sqrt{\left(I_{P(PK)}^2 + I_{P(PK)} \cdot I_{P(VL)} + I_{P(VL)}^2\right) \cdot \frac{D}{3}} \quad \text{(eq. 12)}$$

The turn on switching loss of the main switch is approximated by Equation 13.

$$P_{SW(Qmain)} = \frac{V_{DS} \cdot I_{P(VL)} \cdot t_{SW(on)} \cdot f_{SW}}{6} \quad \text{(eq. 13)}$$

where, $V_{DS}$ is the drain voltage at which the main switch turns on, $t_{sw(on)}$ is the switch turn on time. The main switch turn off switching losses are very small and are ignored.

In an active clamp converter, the main switch achieves Zero−Volt Switching (ZVS) under specific operating conditions. ZVS is affected by input voltage and output load. Even if ZVS is not achieved, reduced voltage switching is obtained. As a first approximation, the input voltage is used as the switch voltage at turn−on for our calculations.

The capacitance at the drain voltage should be minimized to facilitate ZVS. That includes the main and active clamp switches output capacitance ($C_{oss}$) and transformer capacitance. Therefore, $C_{oss}$ should also be considered in addition to the typical $R_{DS(on)}$ and gate charge parameters for the selection of the main switch. Fairchild's FDD2582 is selected for this design as it provides the best tradeoff between $R_{DS(on)}$ and $C_{oss}$. It is a 150 V N−channel MOSFET with an $R_{DS(on)}$ of 58 mΩ.

Using the Design Tool the power dissipation of the main switch at high and low line assuming a 50 ns turn on time is calculated to be 1.49 W and 1.56 W, respectively. Power dissipation of the main switch is dominated at low line by conduction losses and at high line by switching losses. The maximum power dissipation of the main switch is calculated using Equation 14.

$$P = \frac{T_{J(max)} - T_{A(max)}}{R_{\theta JA}} \quad \text{(eq. 14)}$$

where, $R_{\theta JA}$ is the junction to ambient thermal resistance and $T_{J(max)}$ and $T_{A(max)}$ are the maximum junction and ambient temperatures, respectively. Please keep in mind that Equation 14 assumes there are no other heat sources in the system. However, this is not the case in a real system.

As specified in Table 1, $T_{A(max)}$ is 50°C. Solving Equation 14 for $T_{J(max)}$ at high line, a maximum $T_J$ of 131°C is calculated. The maximum allowed $T_J$ is 158°C assuming an 90% derating for $T_{J(max)}$ of the FDD2582.

Power dissipation of the main switch is high and should be verified during design validation to make sure it is still within acceptable limits. However, keep in mind that this is a worst case scenario as the provided $R_{\theta JA}$ does not include airflow. Also, it is for a lower copper weight than the one used on this board.

The thermal resistance of the main switch can be reduced by maximizing the copper area around the package. A heatsink can also be added on top of the package.

### ACTIVE CLAMP SWITCH

The active clamp switch experiences low conduction losses because only the magnetizing current flows through it. Switching losses are negligible because the active clamp switch is turned on after the body diode is conducting.

IR's IRF6217PBF is used for the active clamp switch. It is a 150 V P−channel MOSFET with an on resistance of 2.4 Ω. Only conduction losses are considered for the power dissipation of the active clamp switch. Solving Equation 11, a power dissipation of 0.58 W is calculated for a $T_{J(max)}$ of 79°C.

The designer may be tempted to use a lower on resistance switch to reduce conduction losses. However, this may counterproductive. The active clamp switch has to turn off quickly to divert the magnetizing current and discharge the drain capacitance to achieve ZVS. If not, the magnetizing current will keep flowing through the switch preventing the drain capacitance to be discharged and achieve ZVS. A larger active clamp switch will have lower conduction losses but may increase switching losses on the main switch if ZVS is affected.

The low side active clamp circuit is easier to implement as it is compatible with a ground referenced gate drive signal. However, it requires a negative voltage to turn on the P−channel MOSFET. It is generated using a level shift circuit as the one shown in Figure 1. Active clamp forward converter. It consists of a diode and an ac coupling capacitor ($C_C$). The ac coupling capacitor is selected using Equation 15.

$$C_C = \frac{Q_G}{\Delta V_C} + \frac{V_{DRV} \cdot (1 - D) \cdot D}{\Delta V_C \cdot R_{GS} \cdot f_{SW}} \quad \text{(eq. 15)}$$

where, $Q_G$ is the total gate charge of the switch, $V_{DRV}$ is the gate drive voltage, $\Delta V_C$ is the gate voltage ripple (should be ~ 10% $V_{DRV}$), and $R_{GS}$ is the gate to source resistor. A 0.01 μF is used for a 12 V gate voltage with an $R_{GS}$ of 10 kΩ.

### AUXILIARY SUPPLY REGULATOR

The NCP1562 has an internal startup circuit. It charges the supply capacitor ($C_{AUX}$) on the $V_{AUX}$ pin until the startup threshold is reached. The startup circuit is then disabled and the controller is biased by $C_{AUX}$. The auxiliary capacitor is sized to store enough energy to maintain $V_{AUX}$ above its turnoff threshold, $V_{AUX(off2)}$. An auxiliary supply biases $V_{AUX}$ under normal operating conditions to prevent the converter from turning off.

The auxiliary supply can be generated from a winding on the transformer or on the output inductor. The main difference is the speed at which the supply voltage builds up.

The supply from the transformer builds up quickly where as the output inductor supply builds up with $V_{out}$. However, the output inductor supply is inherently regulated. In this design, the auxiliary supply is implemented from the transformer to reduce the value of $C_{AUX}$. An L−C filter ($L_{AUX}$−$C_{AUX}$) is used to average the voltage from the auxiliary winding as shown in Figure 8.

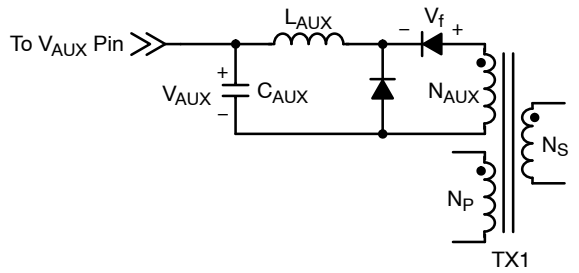


**Figure 8. Auxiliary Supply Architecture**

The number of auxiliary turns ($N_{AUX}$) is calculated using Equation 16.

$$N_{AUX} \approx \left(\frac{V_{AUX}}{DC} + Vf_{SW}\right) \cdot \frac{N_p}{V_{in}} \qquad \text{(eq. 16)}$$

Solving Equation 16, 3.6 turns are required for a $V_{AUX}$ of 12 V and a $V_f$ of 0.7 V. The turns are rounded up to 4 for a $V_{AUX}$ of 13.35 V.

The LC filter averages the voltage as long as the inductor operates in continuous conduction mode. The auxiliary inductor value is selected in the same manner as the output inductor using Equation 6 by replacing the “out” subscript with “AUX”. The auxiliary current ($I_{AUX}$) is calculated using Equation 17.

$$I_{AUX} = I_{AUX3} + f \cdot (Q_{T(main)} + Q_{T(clamp)}) \qquad \text{(eq. 17)}$$

where, $I_{AUX3}$ is the controller bias current (refer to the NCP1562 datasheet) and $Q_{T(main)}$ and $Q_{T(clamp)}$ are the total gate charge of the main and active clamp switches, respectively. Solving Equation 17, an $I_{AUX}$ of 23.2 mA is obtained. The required inductor for an $I_{AUX(min)}$ of 15% of $I_{AUX}$ is 694 μH. Coilcraft’s DO1606T series is selected for the auxiliary inductor. This series is very rugged and has a very low profile. The next size up in the DO1606T series is used. It is 1000 μH.

As previously discussed, $C_{AUX}$ must be sized to maintain $V_{AUX}$ above $V_{AUX(off2)}$ during startup. The NCP1562 reduces the $C_{AUX}$ requirement by turning on the startup circuit if an intermediate threshold ($V_{AUX(off1)}$) is reached. This, in addition to the other factors that affect the auxiliary supply (load current, soft start period, etc.) make the selection of $V_{AUX}$ non trivial. Empirically it was found that 88 μF works well under all operating conditions. However, 116 μF was used as the components were readily available from distribution. The $V_{AUX}$ capacitance consists of one 22 μF ceramic capacitor across the NCP1562 to reduce noise, and two 47 μF tantalum capacitors for bulk storage.

## INPUT FILTER

An input L−C ($L_{in}$−$C_{in}$) filter is used to reduce EMI and provide a solid input voltage to the converter. The input filter design is constrained by stability and power rating criteria.

Oscillation will occur if the converter input impedance, $Z_{in}$, is lower than the filter output impedance, $Z_{out}$. The converter closed loop input impedance is ultimately determined by the converter feedback loop. However, the converter input impedance can be approximated as a negative resistor using 18.

$$Z_{in}(dB\Omega) \approx -20 \log\left(\frac{V_{out}}{I_{out}}\right) \qquad \text{(eq. 18)}$$

The L−C filter output impedance is given by 19.

$$Z_{out}(dB\Omega) \approx L_{in} \parallel \left(n \cdot C_{in} + \frac{R_{ESR}}{n}\right) \qquad \text{(eq. 19)}$$

where, *n* is the number of capacitors in parallel.

The input inductor is selected to handle the converter average input current. Coilcraft’s DS3316P−152 is used as the input inductor.

The input capacitors are selected based on the input ripple current given by 20. Ceramic capacitors are preferred due their low ESR and high ripple current capability. TDK’s C4532X7R2A225MT are used as the input capacitors.

$$I_{in(rms)} = \sqrt{\frac{D}{3}\left(I_{P(VL)}^2 + I_{P(PK)}I_{P(VL)} + I_{P(PK)}^2\right) + \frac{I_{MAG}^2(1-D)}{2}} \qquad \text{(eq. 20)}$$

Equation 20 is an approximation and assumes the magnetizing current reverse directions halfway during the off time. It can be observed that equations 12 and 20 are very similar. The main difference is the ripple component added by the active clamp during the reset of the transformer.

Equation 20 sets the minimum capacitance to comply with the capacitor input ripple current rating. Additional capacitance may be needed to insure the system is stable over the complete operating range.

The input filter is implemented using a 1.5 μH inductor with four 2.2 μF capacitors in parallel. Figure 9 shows the L−C filter output impedance and the approximated converter input impedance over frequency obtained with the Design Tool. As the capacitor ESR changes over frequency, the ESR at the filter corner frequency is used for the analysis.

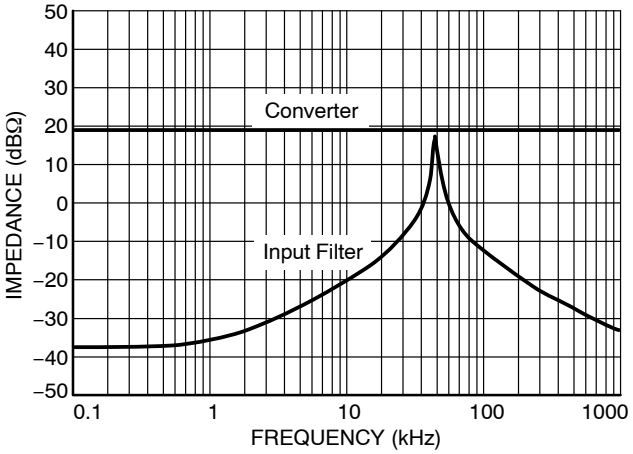


**Figure 9. Input Filter Output Impedance and Approximated Converter Input Impedance**

In general, if the system oscillates, the input filter output impedance can be decreased as in most cases the converter input impedance is dictated by the system specifications. This can be accomplished adding a damping network.

## SYNCHRONOUS RECTIFICATION

Low output voltage converters require synchronous rectification to achieve high efficiency. If a diode is used for rectification, the forward voltage drop becomes a significant portion of the output voltage thus severely affecting the efficiency.

The active clamp topology lends itself for synchronous rectification as it has signals readily available that may be used for driving a synchronous rectifier. The synchronous rectifiers are driven from the main transformer output winding as shown in Figure 10. This configuration is known as self−driven synchronous rectification (SD−SR).

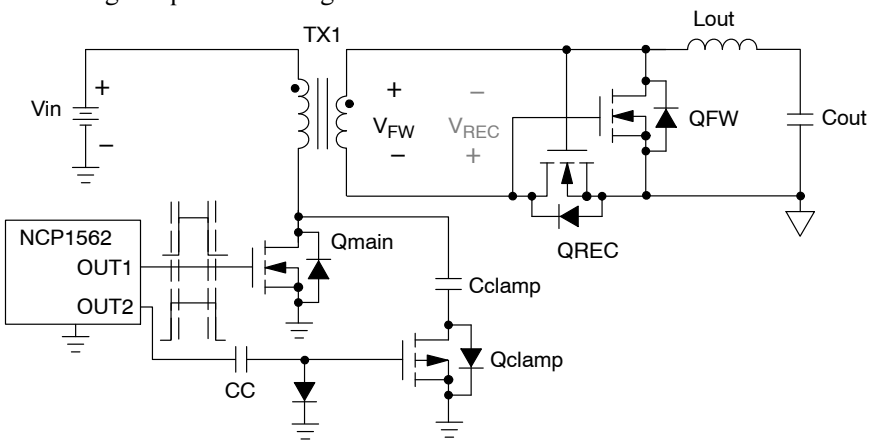


**Figure 10. Synchronous Rectification Circuit**

The voltage of the transformer output when the main switch is on ($V_{FW}$) and off ($V_{REC}$) are given by equations 21 and 22.

$$V_{FW} = \frac{V_{in}}{N} \quad \text{(eq. 21)}$$

$$V_{REC} = \frac{V_{clamp}}{N} \quad \text{(eq. 22)}$$

Before SD−SR can be used, the voltage at the transformer output needs to be calculated to ensure it is high enough to turn on the rectification MOSFETs but it does not exceed its maximum gate voltage. Using the NCP1562 Design Tool the range for $V_{FW}$ and $V_{REC}$ is calculated between 4.7 V and 12.7 V as shown in Figure 11. A MOSFET characterized with a 4.5 V gate voltage should be used to ensure the rectification MOSFET turn on.

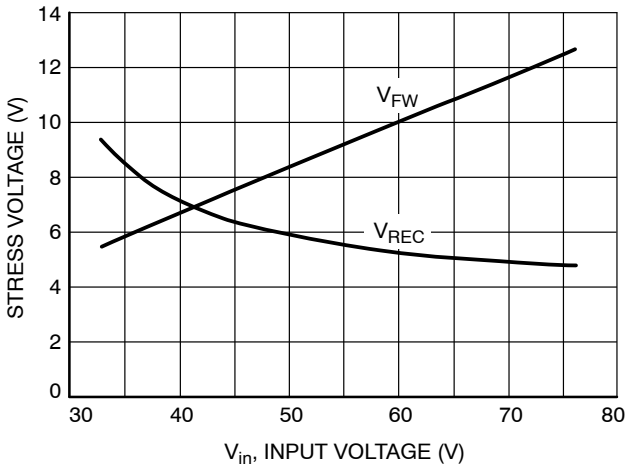


**Figure 11. Synchronous Rectifier Gate Voltage**

If the secondary voltage is not compatible with the MOSFET gate voltage, a few alternatives are available as listed below:

1. Use a lower transformer turns ratio.
2. Add an extra winding or use a stacked winding on the transformer secondary.
3. Drive the MOSFETs from the primary side (OUT1 and OUT2) using a gate drive transformer.

The selection of the rectification MOSFETs in an SD−SR configuration is not trivial. Both conduction and switching losses should be optimized for the best overall efficiency. Contrary to traditional belief, the lowest $R_{DS(on)}$ MOSFET will not always provide the best overall efficiency. The incremental reduction in conduction losses of a low $R_{DS(on)}$ MOSFET may be overcome by an increase in switching losses.

ON Semiconductor's NTMFS4835N is selected for both $Q_{REC}$ and $Q_{FW}$ MOSFETs. It is a 30 V MOSFET with a maximum $R_{DS(on)}$ of 5.0 mΩ and a maximum gate charge of 39 nC at 4.5 V. The NTMFS4835N is housed in a SO−8 Flat Lead (FL) package. The SO−8 FL is a leadless package with an exposed tab to reduce thermal resistance and parasitic inductance and capacitance.

The maximum power dissipation of the SD−SR MOSFETs is calculated using Equation 14. The NTMFS4835 datasheet provides an $R_{\theta JA}$ of 55.1°C/W and a $T_{J(max)}$ of 150°C. Telecom products are usually designed for a $T_{A(max)}$ of 50°C. Solving Equation 14, with 90% derating on $T_{J(max)}$ each MOSFET can dissipate 1.54 W. If higher power dissipation is required, a heatsink can be added to the MOSFET to reduce its $R_{\theta JA}$.

The converter high output current requires multiple MOSFETs to be used in parallel due to the high conduction losses. The number of MOSFETs for $Q_{FW}$ and $Q_{REC}$ is determined by calculating the losses of each one and dividing it by the maximum power dissipation given by Equation 14.

The maximum power dissipation of $Q_{REC}$ occurs at low line and for $Q_{FW}$ at high line. The conduction losses for $Q_{REC}$ and $Q_{FW}$ are given by equations 23 and 24, respectively.

$$P_{cond(REC)} = I_{out(rms)}^2 \cdot D \cdot R_{DS(on)} \quad \text{(eq. 23)}$$

$$P_{cond(FW)} = I_{out(rms)}^2 \cdot (1 - D) \cdot R_{DS(on)} \quad \text{(eq. 24)}$$

The gate charge losses of the driver and body diode conduction losses are given by 25 and 26, respectively.

$$P_{driver} = f_{SW} \cdot Q_{G(TOT)} \cdot V_{gate} \quad \text{(eq. 25)}$$

$$P_{bd} = V_{bd} \cdot I_{out} \cdot f_{SW} \cdot t_{dead} \quad \text{(eq. 26)}$$

Figure 12 shows the synchronous rectification losses calculated by the NCP1562 Design Tool.

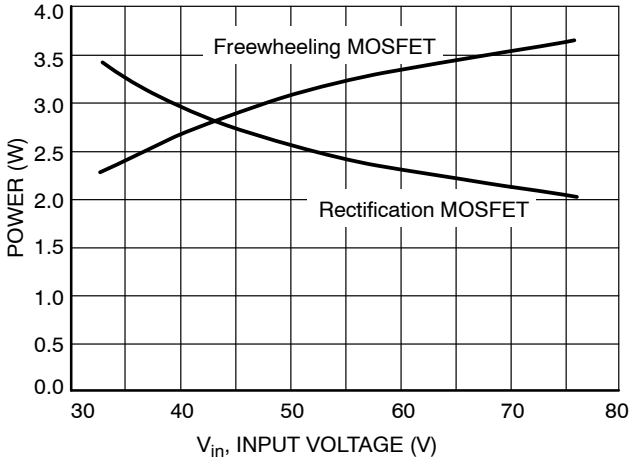


**Figure 12. Synchronous Rectification Losses**

The full load losses for $Q_{FW}$ and $Q_{REC}$ are 3.6 W and 3.4 W, respectively. Two MOSFETs are used in parallel for each of $Q_{FW}$ and $Q_{REC}$. However it is apparent that external cooling or a heatsink is required to deliver full power. Alternatively, a larger number of MOSFETs in parallel could have been used.

Almost no ringing is observed on the drain of the synchronous rectifiers. This is due to the minimum parasitic inductance and capacitance of the SO−8 FL package and the tight layout of the output power stage. No R−C snubbers are required across the synchronous rectifiers.

### OPTOCOUPLER AND $V_{EA}$ CIRCUIT

The output voltage is regulated by comparing the error signal in the $V_{EA}$ pin to the feedforward (FF) ramp. An optocoupler transmits the error signal across the isolation boundary. Typically, optocouplers introduce a pole around 10 kHz. This pole limits the system bandwidth and complicates the frequency compensation of the converter as it occurs at the desired crossover frequency range. The pole is due to the impedance and capacitance at the collector terminal. Fortunately, there are a few tricks to move the optocoupler pole to a higher frequency and increase the system bandwidth.

First, a cascode stage using a bipolar transistor (Q1) is placed between the optocoupler pull up resistor ($R_{EA}$) and the collector of the optocoupler as shown in Figure 13. The collector impedance is now the impedance looking into the emitter of the bipolar transistor which is very small. The optocoupler pole is effectively moved to a higher frequency (> 50 kHz).

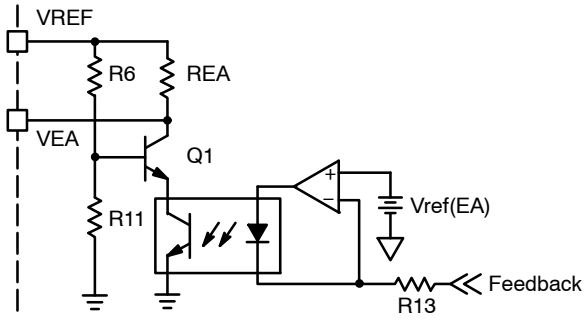


**Figure 13. High Bandwidth Optocoupler Biasing Configuration**

Second, the optocoupler diode is driven with an ideal current source. This arrangement works very well during transients and power up. As the diode is driven with a current instead of a voltage source, the error amplifier output does not have to swing too far during a transient. This arrangement is also immune to supply voltage variations.

The optocoupler gain changes with its bias current, $I_{opto}$. It is not uncommon for an optocoupler to have a gain variation of 10 or more over the operating current range. As the optocoupler bias current changes from low to high line, it presents a design challenge. In addition, optocoupler performance changes with age and temperature. A low gain optocoupler is preferred to minimize its impact in the overall system gain. NEC's PS2703−1−M optocoupler is used in this design.

The optocoupler manufacturer recommends biasing the optocoupler at 1 mA. Our optocoupler is designed to operate at 1 mA at nominal input voltage (48 V). However, the bias current at low or high line will be slightly different. Equation 27 relates the duty ratio to optocoupler bias current,

$$R_{EA} = \frac{V_{REF} - (3 \cdot D + 0.9)}{I_{opto}} \quad \text{(eq. 27)}$$

where, $V_{REF}$ is the voltage reference of the controller. The NCP1562 Design Tool suggests a duty ratio of 0.43 at nominal input voltage. Solving 27, an $R_{EA}$ of 2.81 kΩ is suggested. An $R_{EA}$ of 3.01 kΩ is used. The base of the Q1 is biased at approximately 1.5 V using R6 and R11. That insures the optocoupler collector−emitter voltage is kept above its saturation voltage of 0.3 V.

## FEEDBACK LOOP

The converter regulates the output voltage by adjusting the duty ratio using a negative feedback loop. If the loop is not stable, the converter will oscillate. To insure the loop is stable and has adequate transient response, the closed loop response should have a minimum phase margin of 45° under all line and load conditions. This is accomplished by shaping the open loop response using an error amplifier.

The first step is to determine the open loop frequency response of the converter. An active clamp forward converter operating in voltage mode has two poles, $p_{1,2(LC)}$, due to the output LC filter and one zero, $z_{ESR}$, due to the output capacitor series resistance. In addition it has two complex zeros introduced by the active clamp network. The complex zeros are not shown due to their great complexity. The complex zeros happen before the system poles $P_{1,2(AC)}$. The system crossover frequency should be selected below $P_{1,2(AC)}$ to avoid the complex poles. Equations 28 through 30 show the system poles and zeros.

$$P_{1,2(LC)} = \frac{1}{2\pi\sqrt{L_{out} \cdot C_{out}}} \quad \text{(eq. 28)}$$

$$Z_{ESR} = \frac{1}{2\pi \cdot R_{ESR} \cdot C_{out}} \quad \text{(eq. 29)}$$

$$P_{1,2(AC)} = \frac{(1 - D)}{2\pi\sqrt{L_{MAG} \cdot C_{clamp}}} \quad \text{(eq. 30)}$$

The ESR of the output capacitors is very low (<1 mΩ), pushing $Z_{ESR}$ above 100 kHz. The worst case of the active clamp RHP is at low line. In this design it is around 41.1 kHz.

The controller or modulator gain, $G_{MOD}$, is given by 31.

$$G_{MOD} = \frac{R_{FF} \cdot f_{SW} \cdot C_{FF}}{N} \quad \text{(eq. 31)}$$

Using the values calculated earlier $G_{MOD}$ is 1.86 dB. The gain of the optocoupler is given by 32.

$$G_{OPTO} = \frac{R_{EA} \cdot CTR}{R_{13}} \quad \text{(eq. 32)}$$

where, CTR is the optocoupler transfer ratio, $R_{13}$ is the resistor at the optocoupler anode. Assuming a CTR of 1 the gain is 18.7 dB.

The controller gain and system poles and zeros are listed in Table 2. The simulated open loop frequency response is shown in Figure 14. The simulated frequency response does not show the complex zeros or $P_{1,2(AC)}$ as they are dependent on the operating conditions.

**Table 2. SYSTEM POLES AND ZEROS**

| Parameter | Frequency (kHz) | Magnitude (dB) |
|---|---|---|
| $p_{1,2(LC)}$ | 5.6 | – |
| $z_{(ESR)}$ | > 200 | |
| $p_{1,2(AC)}$ | 41.1 | – |
| $G_{MOD}$ | – | 1.86 |
| $G_{OPTO}$ | – | 18.7 |

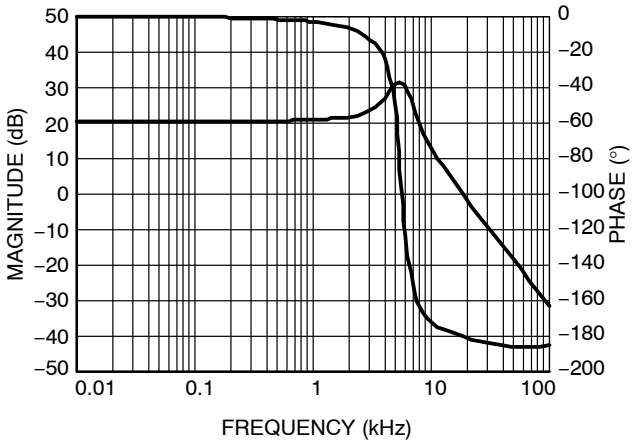


**Figure 14. Simulated Open Loop Frequency Response**

The maximum achievable bandwidth is limited by $p_{1,2(AC)}$ at low line. Therefore, the system crossover frequency, $f_{CO}$, should be set lower than $p_{1,2(AC)}$. In this design, $f_{CO}$ is set at 20 kHz.

Several EA configurations are available. A type II error amplifier, as the one shown in Figure 15, is used in this design as it provides adequate phase margin. A type II error amplifier has 2 poles and 2 zeros. The first pole is at the origin. The frequency of the remaining pole and zeros are calculated using 33 through 35.

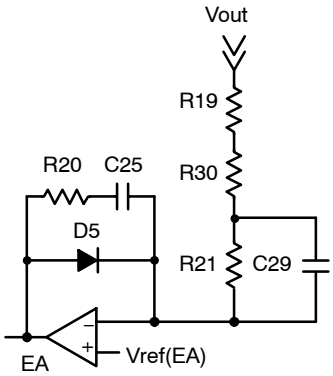


**Figure 15. Type II Error Amplifier**

$$f_{p2} = \frac{1}{2\pi \cdot C_{29} \cdot (R_{21} \parallel R_{30})} \quad \text{(eq. 33)}$$

$$f_{z1} = \frac{1}{2\pi \cdot C_{29} \cdot R_{21}} \quad \text{(eq. 34)}$$

$$f_{z2} = \frac{1}{2\pi \cdot C_{25} \cdot R_{20}} \quad \text{(eq. 35)}$$

Resistor R19 is added to provide an injection point to measure the frequency response. A small resistor value (10 to 20 Ω) is used for R19 so it does not affect the dc operating point. Diode D5 clamps the output of the error amplifier during startup to improve the transient response.

The selection of the compensation network components begins by determining the error amplifier gain, $G_{EA}$, using 36.

$$G_{EA} = 20 \cdot \log\left(\frac{R_{20}}{R_{21}}\right) \quad \text{(eq. 36)}$$

The system open loop gain in Figure 14 Simulated Open Loop Frequency Response at the desired crossover frequency of 15 kHz is 5 dB. Therefore, the EA gain is set at −8.77 dB to achieve a gain of 0 dB at approximately 15 kHz. Resistors R20 and R21 are set at 5.9 kΩ and 16.2 kΩ, respectively. One compensation zero is placed before and one after $p_{1,2(LC)}$ at 482 Hz and 9.8 kHz, respectively. Capacitors C25 and C29 are set at 0.056 μF and 1000 pF, respectively. The second pole is set at a 457 kHz setting R30 at 348 Ω. The simulated frequency response is shown in Figure 16. The simulated crossover frequency is around 15 kHz with a 60° phase margin.

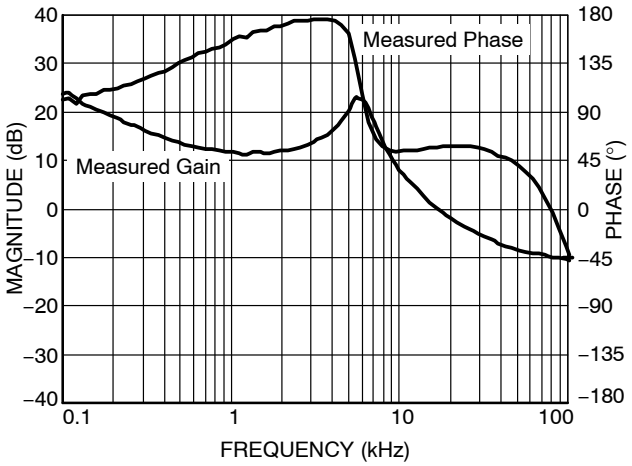


**Figure 16. Simulated System Frequency Response**

## ERROR AMPLIFIER VOLTAGE REFERENCE

The error amplifier reference voltage ($V_{ref(EA)}$) is generated using On Semiconductor's TLV431 as shown in Figure 17.

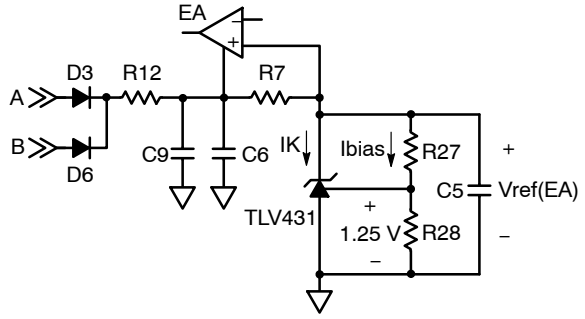


**Figure 17. Error Amplifier Reference Voltage**

The error amplifier reference voltage is set at 3.3 V using R27 and R28. This eliminates the need of a bias resistor between the EA inverting input and ground.

The voltage across R28 is regulated at 1.25 V by the TLV431. Assuming a bias current ($I_{bias}$) of 500 μA, R28 is set at 2.49 kΩ. Resistor R27 is set by calculating the difference between $V_{ref(EA)}$ and 1.25 V and dividing it by $I_{bias}$. It is set at 4.22 kΩ. Capacitor C5 provides noise immunity for $V_{ref(EA)}$. It is set at 1000 pF.

The maximum voltage of either A or B provides the voltage supply for the EA and the TLV431. Signals A and B are taken from the dot (A) and non−dot (B) ends of the secondary winding of the main transformer. The NCP1562 Design Tool shows a minimum voltage of approximately 7 V. The maximum value of R7 is calculated using 37.

$$R7 = \frac{V_{(A\ or\ B)} - 0.7\ V}{I_K + I_{bias}} \qquad \text{(eq. 37)}$$

where, $V_f$ is the diode drop of D3 or D6 and $I_K$ is the TLV431 minimum cathode current. Solving 37 with an $I_K$ of 80 μA sets the maximum value of R7 at 10.9 kΩ. The value of R7 is set at 4.22 kΩ.

The switching noise at nodes A and B is attenuated by placing a small resistor (R12) in series with D3 and D6. The value of R12 is set at 49.9 Ω. The components of the peak detector (D3, D6, R12 and C9) are placed close to each other but away from the EA to keep noise low. A bypass capacitor (C6) is placed across the supply terminals of the EA. Both C9 and C6 are set at 0.1 μF.

## CURRENT LIMIT CIRCUIT

This converter is designed to deliver 100 W under normal operating conditions. However, under a fault condition the current may increase significantly and permanently damage the system. The NCP1562 incorporates an extremely accurate current limit circuit to protect the system while a current limit condition is present. A low propagation delay combined with an extremely accurate current limit threshold limit the maximum power delivered under a current limit condition. This allows the designer to have a robust and safe system without excessive over design.

The NCP1562 has two overcurrent protection methods, cycle by cycle and cycle skip. In cycle by cycle, the conduction period ends once the current limit threshold is reached. Cycle skip is enabled if the converter is in a continuous current limit for a user programmed time. While in cycle skip mode, the converter power downs and restart after a user determined time.

The NCP1562A is used in this design. It has a current limit voltage threshold, $V_{ILIM}$, of 0.2 V. A current sense resistor is used to reduce system cost and complexity. It is calculated using 38.

$$R_{sense} = \frac{V_{ILIM}}{I_{P(PK)}} \qquad \text{(eq. 38)}$$

Using $I_{P(PK)}$ calculated earlier, $R_{sense}$ is calculated at 34 mΩ. The value of the sense resistor is set at 33 mΩ.

The NCP1562 incorporates a 75 ns leading edge blanking circuit to mask the leading edge spike of the current signal. The demo board also provides external blanking time using a simple RC low pass filter comprised of R10 and C11. The cutoff frequency of the low pass filter is selected several orders of magnitude greater than the operating frequency to avoid distortion of the current sense signal. The value of R10

is set at 100 Ω and C11 is set at 100 pF. The complete current sense circuit is shown in Figure 18.

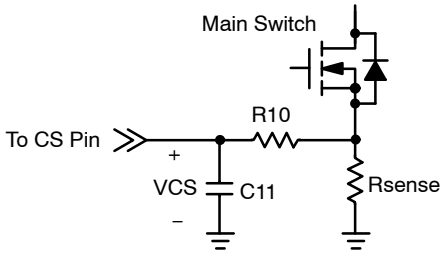


**Figure 18. Current Sense Circuit**

The converter enters the cycle skip current mode if a continuous over current condition is exists. Once a current limit event is detected, a 90 μA current source begins charging the capacitor on the CSKIP pin. If the capacitor charges to 3 V, the converter enters a soft stop mode. A cycle skip period of 330 μs is set with a 0.01 μF capacitor.

## UNDER AND OVER VOLTAGE DETECTOR

The NCP1562 facilitates design by incorporating tightly controlled undervoltage (UV) detector. In addition, it incorporates an independent overvoltage (OV) detector in the same pin. The pin is biased using a resistor divider as shown in Figure 19.

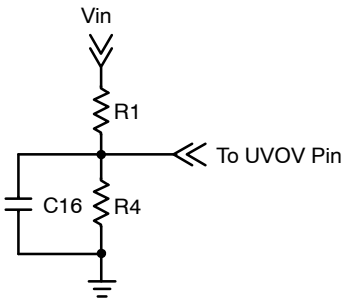


**Figure 19. UVOV Bias Circuit**

The minimum operating voltage of the system is controlled by comparing the voltage on the UVOV pin to a 2 V reference, $V_{OV}$. The system turn on threshold, $V_{in(UV)}$, is determined by the ratio of the resistor divider on the UV pin as shown in equation 39.

$$V_{in(UV)} = V_{UV} \cdot \frac{(R_1 + R_4)}{R_4} \qquad \text{(eq. 39)}$$

The maximum operating voltage, $V_{in(OV)}$, is controlled by comparing the voltage on the UVOV pin to an internal 3 V reference, $V_{OV}$. An internal current source ($I_{offset(UVOV)}$) sinks 50 μA into the UVOV pin once the UVOV voltage exceeds 2.5 V. The voltage offset introduced by this current source allows independent adjustment of $V_{in(UV)}$ and $V_{in(OV)}$ (patent pending). The OV threshold depends on the ratio of the resistor divider as well as the absolute value of R1 as shown in equation 40.

$$V_{in(OV)} = V_{OV} \cdot \frac{(R_1 + R_4)}{R_4} + (I_{offset(UVOV)} \cdot R1) \qquad \text{(eq. 40)}$$

A small capacitor of at least 1000 pF is required on the UVOV to provide noise immunity and filter turn ON and turn OFF transitions on the input line.

The Design Tool suggests using an R1 of 504 kΩ and an R2 of 32.4 kΩ. Used values are 523 Ω and 32.4 kΩ for R1 and R4, respectively. The calculated operating voltage range is between 35.31 V and 80.15 V with $V_{in}$ increasing and between 32.52 V and 75 V with $V_{in}$ decreasing.

## MAXIMUM DUTY RATIO

As shown in Figure 4, the drain voltage of the main switch of an active clamp converter increases rapidly at low input voltages. Accurate duty ratio control allows the designer to fully optimize the system without risking exceeding the voltage rating of the main switch.

The NCP1562 incorporates an extremely accurate duty ratio control. It is trimmed during manufacturing to achieve better that ±5% accuracy over the complete temperature and process range.

Duty ratio and frequency are controlled using a timing resistor, $R_T$, and capacitor, $C_T$, on the RTCT pin. The resistor is connected between the VREF and RTCT pins and the capacitor is connected between the RTCT and GND pins.

The converter is designed to operate at 350 kHz with a maximum duty ratio of 63%. Taking into account the overlap time delay, the required oscillator duty ratio is 66%. The Design Tool suggests initial values for $R_T$ and $C_T$ of 14.5 and 320 pF, respectively. Final values of $R_T$ and $C_T$ are set at 15 kΩ and 300 pF.

## VOLT SECOND LIMIT AND FEEDFORWARD

A forward converter regulates the output voltage by maintain a constant Volt−second (V−sec) product. If the maximum V−sec product is exceeded, the transformer will saturate and possibly damage to the system. Therefore, it is critical to accurately control the V−sec product in a forward converter.

The NCP1562 implements V−sec limit by generating a Feedforward (FF) Ramp proportional to $V_{in}$ and comparing it to a 3 V reference. The ramp is generated by charging an external capacitor ($C_{FF}$) with a resistor ($R_{FF}$) from $V_{in}$. Feedforward is achieved by changing the slope of the FF Ramp while maintaining a constant error voltage. Feedforward reduces line voltage variations and provides a frequency gain independent of $V_{in}$ making the system easier to compensate.

The peak voltage of the ramp is set below 3 V under normal operating conditions. The margin allows the converter to quickly respond during a transient.

The FF components are calculated starting with the desired maximum FF charge current, $I_{FF}$. Given $I_{FF}$, $R_{FF}$ is calculated by dividing the maximum input voltage by $I_{FF}$. The FF capacitor is calculated using 41.

$$C_{FF} = \frac{I_{FF} \cdot V - sec_{(max)}}{3\ V} \qquad \text{(eq. 41)}$$

Our transformer has a V−sec$_{(max)}$ of 62.4 V−μsec. Selecting an arbitrarily $I_{FF}$ of 1.75 mA, the Design Tool suggest values of 43.4 kΩ and 479 pF for $R_{FF}$ and $C_{FF}$, respectively. Final values are 45.3 kΩ for $R_{FF}$ and 470 pF for $C_{FF}$. As duty ratio control is very important, the tolerances for $R_{FF}$ and $C_{FF}$ are set at 1% and 5%, respectively.

### SOFT−START

Soft−start slowly starts the converter and reduces stress during power up. The NCP1562 implements soft−start by comparing the voltage in the SS pin to the FF Ramp.

Soft−start is adjusted by placing an external capacitor, $C_{SS}$, between the SS pin and ground. The capacitor is charged with a constant 10 μA current source. The peak voltage of the FF Ramp is 3 V. Therefore, soft−start ends once the SS voltage exceeds the FF Ramp or it exceeds 3 V. Under steady state conditions the SS capacitor is charged to 3.8 V.

### SOFT−STOP

The clamp capacitor in a forward topology needs to be discharged while powering down the converter. If the capacitor remains charged after power down it may damage the converter. First, the resonant tank between $C_{clamp}$ and $L_{MAG}$ used for ZVS during normal operation will continue to resonate after power down as long as energy is stored in the capacitor. Second, a long reset time is applied to the transformer during power up as duty ratio slowly increases from 0%. If the capacitor is charged during power up, the maximum V−sec of the transformer may be exceeded. This will push the transformer far into the third quadrant of the B−H curve, possibly saturating the transformer.

The NCP1562 solves these problems by using a novel approach called soft−stop. Soft−stop reduces the duty ratio until it reaches 0% prior to turn off. Duty ratio is reduced by discharging the capacitor on the SS pin using a 90 μA current source. The voltage of the clamp capacitor is given by 42. It can be observed that the clamp capacitor voltage will approach zero as duty ratio approaches zero.

$$V_{clamp} = \frac{V_{in} \cdot D}{1 - D} \qquad \text{(eq. 42)}$$

Empirically it is determined that a 0.1 μF is sufficient to discharge the clamp capacitor under all operating conditions. The worst case condition for soft−stop is light load at high line. During this condition, $V_{EA}$ is at its lowest making the achievable soft−stop time a minimum for a given capacitance. Figure 20 shows the drain of the main switch during power down at high line and no load. As expected, soft−stop provides a controlled turn off without any unwanted oscillations on the drain voltage.

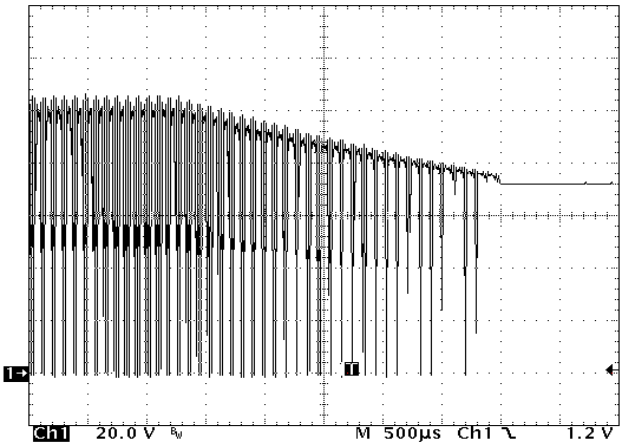


**Figure 20. Converter Power Down using Soft−Stop**

The same capacitor is used for soft−start and soft−stop. The minimum soft−start time is determined by the required soft−stop period. A soft−start to soft−stop ratio of 1/10 is set with the internal charge and discharge currents. If a different ratio is required, a resistor can be placed between the $V_{REF}$ and SS pins to increase the SS charge current.

### BOARD LAYOUT

The converter is built to validate the design using a 4 layer FR4, double sided board. The converter meets the industry standard half brick (2.3 in. x 2.4 in.) footprint and pinout. Power components are placed on the top layer (primary) and control components on the bottom (secondary) layer. The board is constructed using 2 oz copper. The top and bottom layers are plated to 3 oz. to improve power dissipation. The two inner layers are used for ground and signal routing.

During the layout process care was taken to:

1. Minimize trace length, especially for high current loops.
2. Use wide traces for high current connections.
3. Use a single ground connection.
4. Keep sensitive nodes away from noisy nodes such as drain of power switches.
5. Place decoupling capacitors close to ICs.
6. Sense output voltage at the output terminal to improve load regulation.

The layers are numbered 1 through 4 from top to bottom and are shown in Figure 21 through Figure 24. The top and bottom layers show the component location.

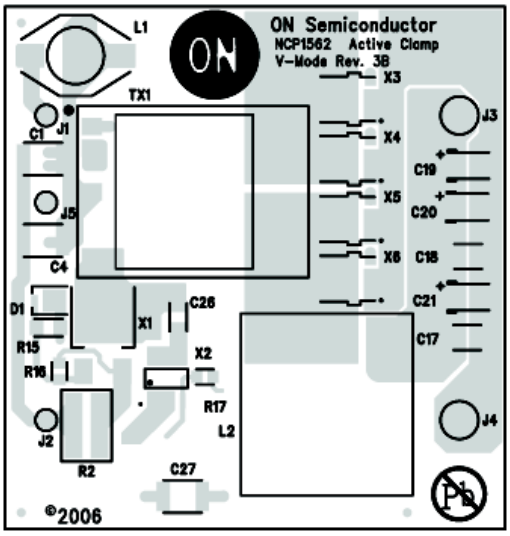


Figure 21. Layer 1 (Top)

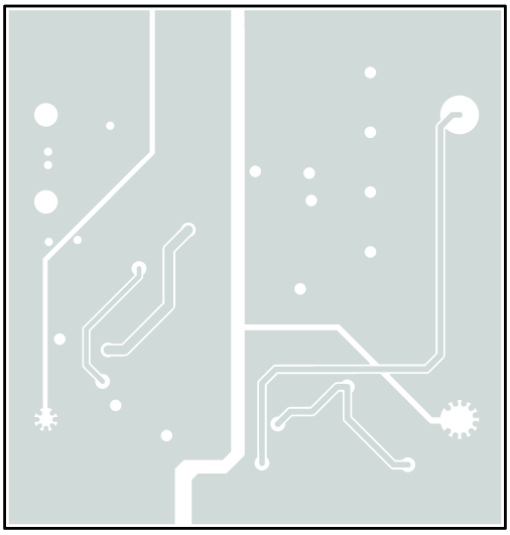

Figure 23. Inner Layer 3

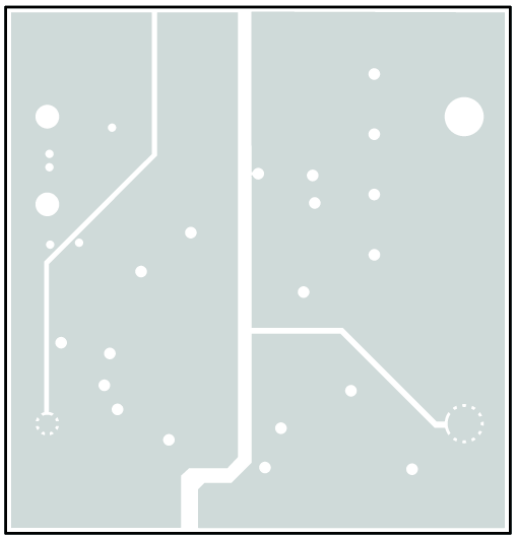

Figure 22. Inner Layer 2

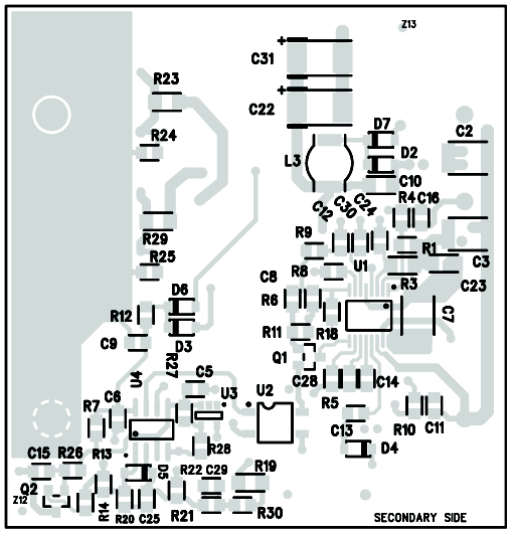


Figure 24. Layer 4 (Bottom)

The layout files may be available. Please contact your sales representative for availability.

## DESIGN VALIDATION

The top and bottom view of the board are shown in Figure 25 and Figure 26, respectively.

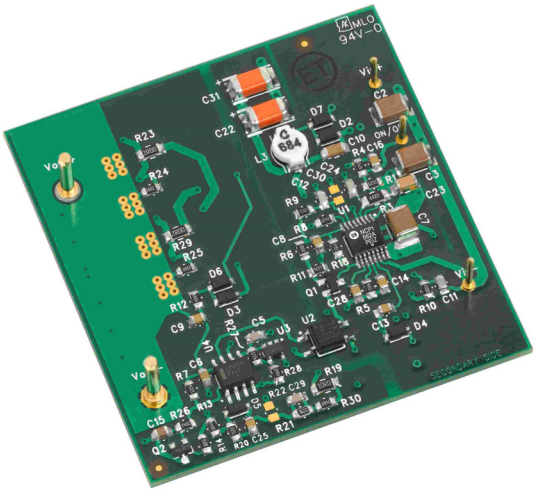

**Figure 25. NCP1562 Demo Board Top View**

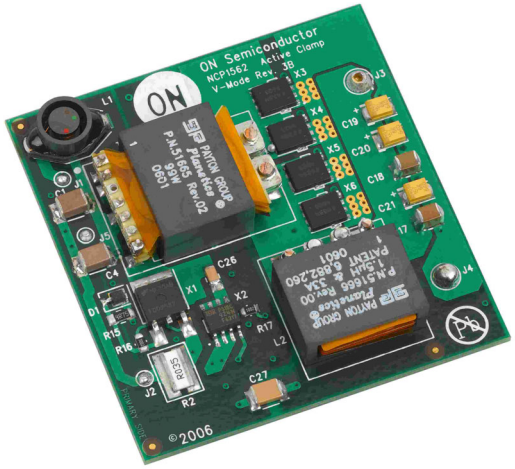


**Figure 26. NCP1562 Demo Board Bottom View**

The circuit schematic is shown in Figure 27 and the bill of material is listed in Table 3.

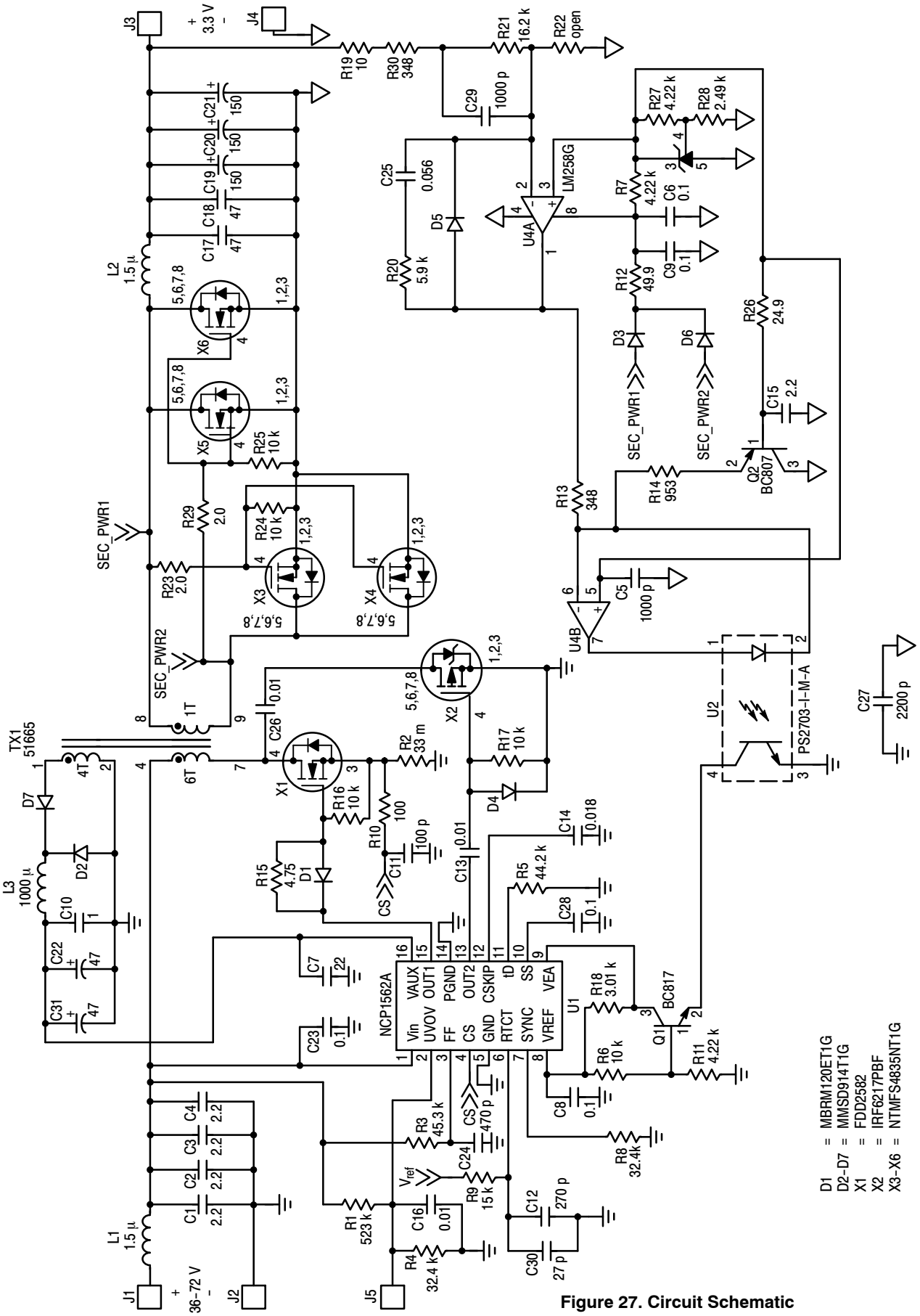


**Figure 27. Circuit Schematic**

**Table 3. BILL OF MATERIALS**

| Reference | Value | Part | Vendor | Comments |
|---|---|---|---|---|
| C1−C4 | 2.2 | C4532X7R2A225MT | TDK | 100 V |
| C5,C29 | 1000 p | VJ0805A102JXAAT | Vishay | 50 V |
| C6,C8,C9,C28 | 0.1 | VJ0805Y104KXAAT | Vishay | |
| C7 | 22 | C4532X5R1C226M | TDK | 16 V |
| C10 | 1 | C3216X7R1E105M | TDK | 25 V, 20% |
| C11 | 100 p | VJ0805A101KXAAT | Vishay | |
| C12 | 300 p | VJ0805A301JXAAT | Vishay | If not Available, use 270 pF |
| C13,C16 | 0.01 | VJ0805Y103KXAAT | Vishay | |
| C14 | 0.018 | VJ0805Y183KXAAT | Vishay | |
| C15 | 2.2 | C2012X5R1A225K | TDK | |
| C17,C18 | 47 | C3225X5R0476M | TDK | 6.3 V |
| C19,C20,C21 | 150 | T520B157M006ATE045 | Kemet | 6.3 V |
| C22, C31 | 47 | 595D476X9016C2T | Vishay | 16 V |
| C23 | 0.1 | C3216X7R2A104K | TDK | 100 V |
| C24 | 470 p | VJ0805A471JXAAT | Vishay | |
| C25 | 0.056 | VJ0805Y563KXXAT | Vishay | 10% |
| C26 | 0.01 | C3216X7R2J103M | TDK | 630 V |
| C27 | 2200 p | C4532X7R3D222K | TDK | 2000 V |
| C30 | 27 p | VJ0805A270JXAAT | Vishay | Use only if C12 is 270 pF |
| D1 | | MBRM120ET1G | ON Semiconductor | 20 V, 1 A Schottky |
| D2−D7 | | MMSD914T1G | ON Semiconductor | 100 V Diode |
| J1,J2,J5 | | 3103−2−00−21−00−00−08−0 | Mill−Max | 40 mils |
| J3,J4 | | 3231−2−00−34−00−00−08−0 | Mill−Max | 80 mils |
| L1 | 1.5 μ | DS3316P−152 | Coilcraft | Input Choke |
| L2 | 1.5 μ | 51666 | Payton | Output Choke |
| L3 | 1000 μ | DO1606T−105 | Coilcraft | Aux. Supply Choke |
| R1 | 523 k | CRCW0805523KFKEA | Vishay | |
| R2 | 0.035 | LRC−LRF3WLF−01−R033−F | IRC Electronics | Current Sense R |
| R3 | 45.3 k | CRCW120645K3FKEA | Vishay | 0.25 W |
| R4, R8 | 32.4 k | CRCW080532K4FKEA | Vishay | |
| R5 | 44.2 k | CRCW080544K2FKEA | Vishay | |
| R9 | 15 k | CRCW080515K0FKEA | Vishay | |
| R10 | 100 | CRCW0805100RFKEA | Vishay | |
| R7, R11, R27 | 4.22 k | CRCW08054K22FKEA | Vishay | |
| R12 | 49.9 | CRCW080549R9FKEA | Vishay | |
| R13, R30 | 348 | CRCW0805348RFKEA | Vishay | |
| R14 | 953 | CRCW0805953RFKEA | Vishay | |
| R15 | 4.75 | CRCW12064R75FKEA | Vishay | |
| R6, R16−R17, R24−R25 | 10 k | CRCW080510K0FKEA | Vishay | |
| R18 | 3.01 k | CRCW08053K01FKEA | Vishay | |
| R19 | 10 | CRCW120610R0FKEA | Vishay | |
| R20 | 5.9 k | CRCW08055K90FKEA | Vishay | |
| R21 | 16.2 k | CRCW08051622FKEA | Vishay | |
| R22 | open | CRCW0805... | Vishay | |
| R23,R29 | 2.00 | CRCW12062R00FKEA | Vishay | |
| R26 | 24.9 k | CRCW080524K9FKEA | Vishay | |
| R28 | 2.49 k | CRCW08052K49FKEA | Vishay | |
| TX1 | | 51665 | Payton | Power Tx |
| U1 | | NCP1562ADBR2G | ON Semiconductor | Controller |
| U2 | | PS2703−1−M−A | NEC | Optocoupler |
| U3 | | TLV431ASNT1G | ON Semiconductor | Shunt Reference |
| U4 | | LM258DG | ON Semiconductor | Op Amp |
| X1 | | FDD2582 (*SUD25N15−52) | Fairchild (Vishay) | 150 V MOSFET |
| X2 | | IRF6217PBF | IR | 150 V PFET |
| X3−X6 | | NTMFS4835NT1G | ON Semiconductor | 30 V MOSFET |
| Q1 | BC817−25 | BC817−25LT1G | ON Semiconductor | npn transistor |
| Q2 | BC807−25 | BC807−25LT1G | ON Semiconductor | pnp transistor |

*Alternate Part number

1. TDK components can be ordered at (847) 803−6100.
2. Vishay Components can be ordered at (402) 563−6866.
3. Payton components can be ordered at (561) 989−9585 ext. 13.
4. Kemet components can be ordered at (480) 831−2151.

The converter performance is evaluated and compared to our original goals. The evaluation criteria includes:

1. Open loop frequency response.
2. Efficiency.
3. Line and load regulation.
4. Step load response.
5. Output voltage ripple.

The open loop response is measured injecting an AC signal across R19 using a network analyzer and an isolation transformer as shown in Figure 28. The open loop response is the ratio of B to A.

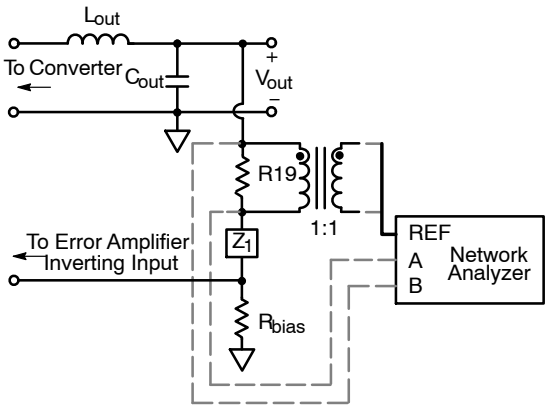


**Figure 28. Open Loop Frequency Response Measurement Setup**

The measured and calculated open loop responses are shown in Figure 29. The measured phase margin is 57° and the crossover frequency is 16.7 kHz. A good correlation is observed between the simulated and calculated responses up to around 30 kHz. The simulated tool does not show the complex zeros and $P_{1,2(AC)}$ of the active clamp.

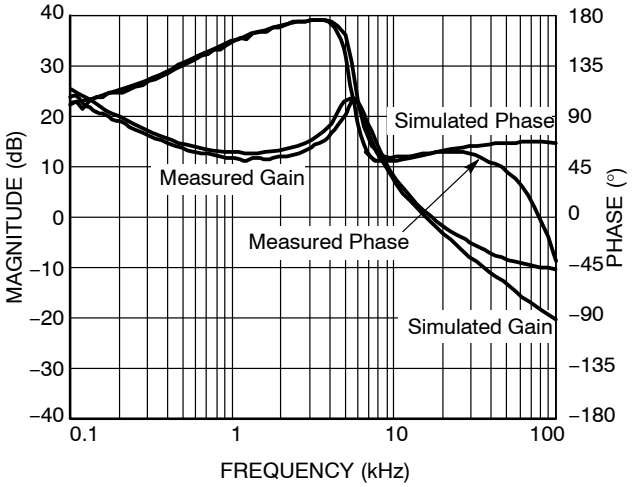


**Figure 29. Measured and Calculated Open Loop Frequency Responses**

The full load efficiency of the converter is measured above 91% across the complete input voltage range. Figure 30 shows the efficiency vs output current at 36 V, 48 V and 72 V. The peak efficiency is measured at 92.8%.

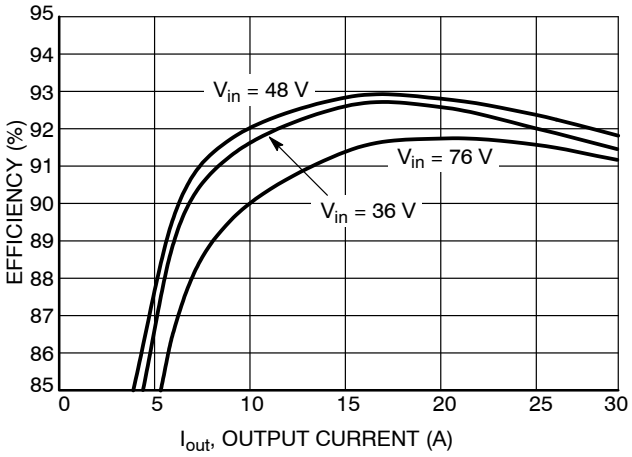


**Figure 30. Efficiency vs. Output Current**

Line and load regulation are calculated using 43 and 44, respectively.

$$Reg_{(line)} = \frac{\Delta V_{out}}{\Delta V_{in}} \quad \text{(eq. 43)}$$

$$Reg_{(load)} = \frac{V_{out(no\ load)} - V_{out(full\ load)}}{V_{out(no\ load)}} \quad \text{(eq. 44)}$$

Line regulation is measured below 0.01% and load regulation is measured below 0.23%.

The dynamic response of the converter at 48 V is evaluated stepping the load current from 50% to 75% and from 75% to 50% of $I_{out(max)}$. The step load response is shown in Figure 31.

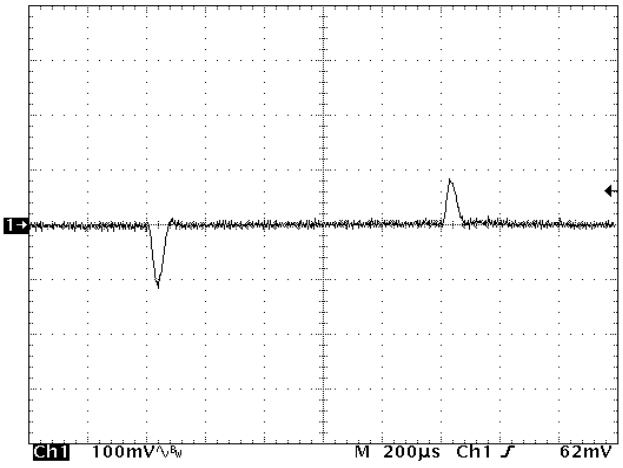


**Figure 31. Output Voltage Response to a Step Load from 22.5 A to 15 A.**

The output voltage ripple is measured at 16 mV at high line and full load. It is significantly below the 50 mV target. The output voltage ripple waveform at high line and full load is shown in Figure 32.

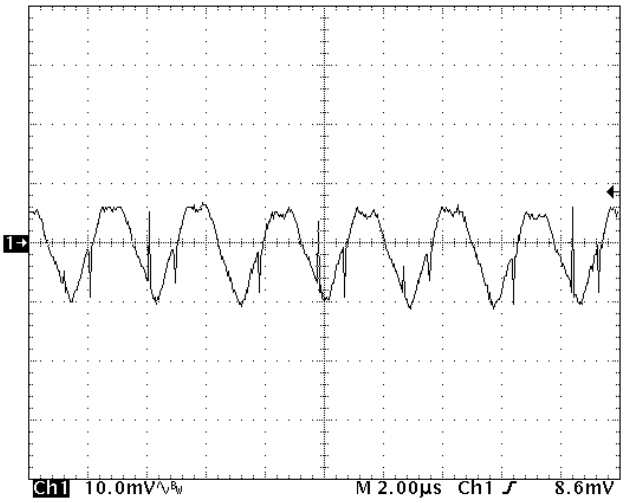


**Figure 32. Output Voltage Ripple at High Line and Full Load**

## THERMAL PERFORMANCE

This demo board is designed to operate with airflow as in a telecom system. Airflow is required if the converter operates above 50% of its rated power. Optimum cooling is achieved when air flows from the output side to the input side.

The thermal performance of the board is evaluated using an infrared camera. Figure 33 through Figure 36 show several images of the board at full load. Images include top and bottom layers at low and high line. All images were taken with airflow from the output side to the input side.

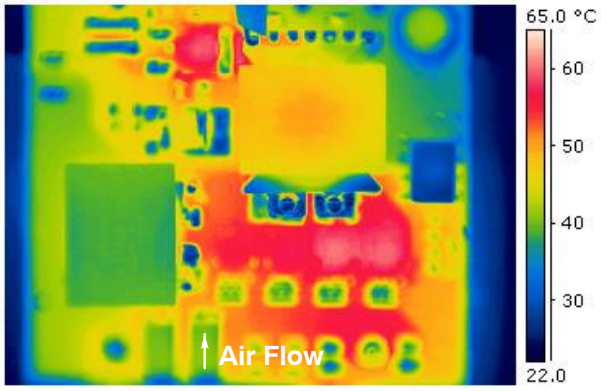


**Figure 33. Thermal Image of the Top of the Board at Low Line and Full Load Condition**

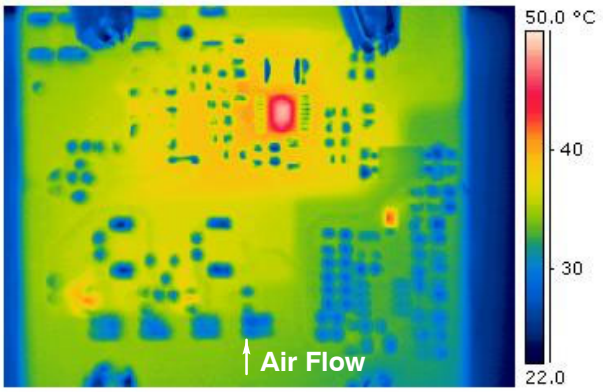


**Figure 34. Thermal Image of the Bottom of the Board at Low Line and Full Load Condition**

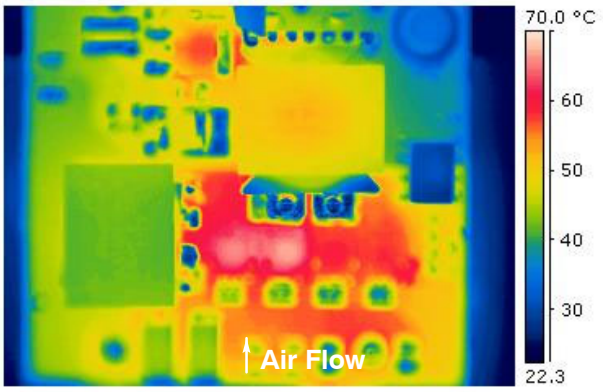


**Figure 35. Thermal Image of the Top of the Board at High Line and Full Load Condition**

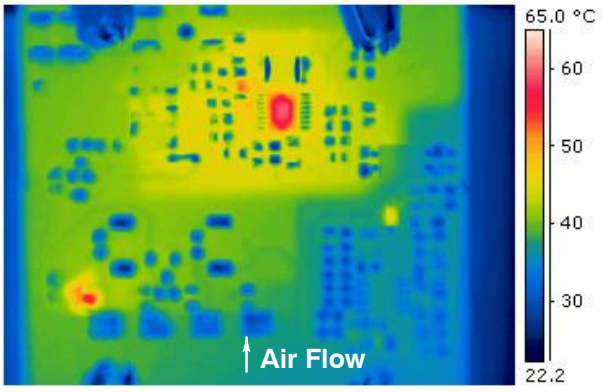


**Figure 36. Thermal Image of the Bottom of the Board at High Line and Full Load Condition**

Most of the losses on the board are on the main switch and synchronous rectifiers. The synchronous rectifier losses are dominated by conduction losses. At low line, $Q_{FW}$ has the higher duty ratio and thus the higher power dissipation as shown in Figure 33. At high line, $Q_{REC}$ has the higher duty ratio and thus the higher power dissipation as shown in Figure 35.

The NCP1562 demo board thermal performance can be optimized by using heatsinks, integrating magnetic components on the board, using additional layers and placing the synchronous rectifiers farther away from each other.

Please keep in mind that this is a demonstration board to showcase the flexibility of the NCP1562. A commercially available dc−dc converter will use advanced packaging and manufacturing techniques to maximize power dissipation of critical components.

## SUMMARY

A 100 W converter is designed and built using the active clamp forward topology. The converter is implemented using the NCP1562. The full load efficiency is measured above 91% over the complete operating range.

The converter provides excellent transient response. Output voltage ripple is measured at 16 mV. Phase margin and crossover frequency are measured at 57° and 16.7 kHz, respectively.

This demo board is designed to demonstrate the features and flexibility of the NCP1562. This design should not be used for production or manufacturing purposes.

## REFERENCES

1. Pressman, Abraham I. Switching Power Supply Design. 2nd ed. New York, NY: MacGraw Hill.

2. Ridley, Ray. “The Evolution of Power Electronics.” Switching Power Magazine.

3. High Performance Active Clamp/Reset PWM Controller Datasheet NCP1562, www.onsemi.com.

4. Dhaval Dalal and Larry Wofford, “Novel Control IC for Single Ended Active−Clamp Converters,” in HFPC’95 Conf. Proc., pp. 136−146, 1995.

5. G. Stojcic, F. Lee and S. Hiti, “Small−Signal Characterization of Active Clamp PWM Converters,” in VPEC Seminar Conf. Proc., pp. 237−245, 1995.

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